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FDS6679AZ P-Channel PowerTrench[®] MOSFET

March 2009

-30V, -13A, 9mΩ

General Description

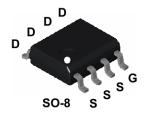
This P-Channel MOSFET is producted using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance.

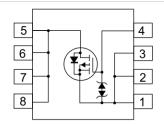
This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.

Features

- Max $r_{DS(on)}$ = 9.3m Ω at V_{GS} = -10V, I_D = -13A
- Max $r_{DS(on)}$ = 14.8m Ω at V_{GS} = -4.5V, I_D = -11A
- Extended V_{GS} range (-25V) for battery applications
- HBM ESD protection level of 6kV typical (note 3)
- High performance trench technology for extremely low ^rDS(on)
- High power and current handing capability
- RoHS Compliant







MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V _{DS}	Drain to Source Voltage		-30	V
V _{GS}	Gate to Source Voltage		±25	V
I _D	Drain Current -Continuous	(Note 1a)	-13	
	-Pulsed		-65	A
	Power Dissipation for Single Operation	(Note 1a)	2.5	
P_D		(Note 1b)	1.2	W
		(Note 1c)	1.0	
T _J , T _{STG}	Operating and Storage Temperature		-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance , Junction to Ambient (Note 1a)	50	°C/W
$R_{\theta JC}$	Thermal Resistance , Junction to Case (Note 1)	25	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
FDS6679AZ	FDS6679AZ	13"	12mm	2500 units

Electrical Characteristics T_J = 25°C unless otherwise noted

Parameter

Off Characteristics						
B _{VDSS}	Drain to Source Breakdown Voltage	$I_D = -250 \mu A, V_{GS} = 0 V$	-30			V
$\frac{\Delta B_{VDSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I_D = -250 μ A, referenced to 25°C		-20		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -24V, V _{GS} =0V			-1	μΑ
IGSS	Gate to Source Leakage Current	$V_{GS} = \pm 25V, V_{DS} = 0V$			±10	μА

Test Conditions

Min

Тур

Max

Units

On Characteristics (Note 2)

Symbol

V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = -250 \mu A$	-1	-1.9	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = -250 μ A, referenced to 25°C		6.5		mV/°C
r _{DS(on)} Drain to So		$V_{GS} = -10V, I_D = -13A$		7.7	9.3	
	Drain to Source On Resistance	$V_{GS} = -4.5V, I_D = -11A$		11.8	14.8	mΩ
	Brain to Source on Resistance	$V_{GS} = -10V, I_D = -13A,$ $T_J = 125$ °C		10.7	13.4	11152
9 _{FS}	Forward Transconductance	$V_{DS} = -5V, I_{D} = -13A$		55		S

Dynamic Characteristics

C _{iss}	Input Capacitance	\\ - 45\\ \\ - 0\\	2890	3845	pF
C _{oss}	Output Capacitance	V _{DS} = -15V, V _{GS} = 0V, f = 1MHz	500	665	pF
C _{rss}	Reverse Transfer Capacitance	1 - 11/11/12	495	745	pF

Switching Characteristics (Note 2)

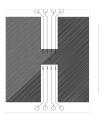
t _{d(on)}	Turn-On Delay Time			13	24	ns
t _r	Rise Time	$V_{DD} = -15V, I_{D} = -1A$ $V_{GS} = -10V, R_{GS} = 6\Omega$		15	27	ns
t _{d(off)}	Turn-Off Delay Time			210	336	ns
t _f	Fall Time			92	148	ns
Qg	Total Gate Charge	$V_{DS} = -15V, V_{GS} = -10V,$ $I_{D} = -13A$		68	96	nC
Qg	Total Gate Charge	15//// 5//		38	54	nC
Q _{gs}	Gate to Source Gate Charge V _{DS} = -15V, V _{GS} = -5V, I _D = -13A			10		nC
Q_{gd}	Gate to Drain Charge	10 - 10/4		17		nC

Drain-Source Diode Characteristic

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0V, I_{S} = -2.1A$	-0.7	-1.2	V
t _{rr}	Reverse Recovery Time	$I_F = -13A$, di/dt = 100A/ μ s		40	ns
Q _{rr}	Reverse Recovery Charge	I _F = -13A, di/dt = 100A/μs		-31	nC

Notes

13 R_{0,IA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{0,IC} is guaranteed by design while R_{0,CA} is determined by the user's board design.



a) 50°C/W when mounted on a 1 in² pad of 2 oz copper



b)105°C/W when mounted on a .04 in² pad of 2 oz copper



c) 125°C/W when mounted on a minimun pad

Scale 1: 1 on letter size paper

- 2: Pulse Test:Pulse Width <300µs, Duty Cycle <2.0%
- 3: The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.



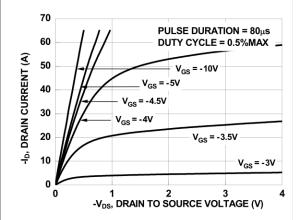


Figure 1. On Region Characteristics

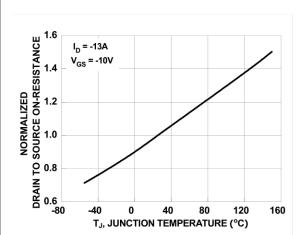


Figure 3. Normalized On Resistance vs Junction Temperature

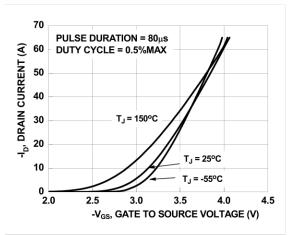


Figure 5. Transfer Characteristics

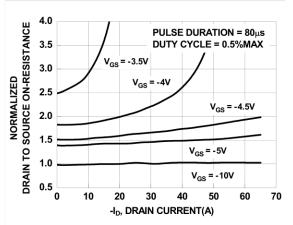


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

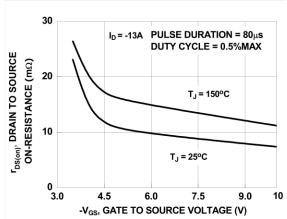


Figure 4. On-Resistance vs Gate to Source Voltage

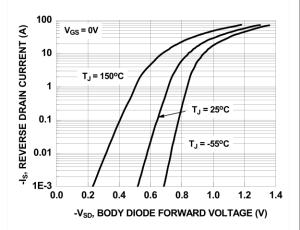


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25°C unless otherwise noted

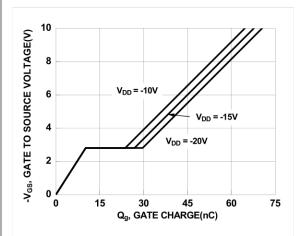


Figure 7. Gate Charge Characteristics

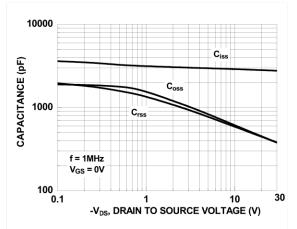


Figure 8. Capacitance vs Drain to Source Voltage

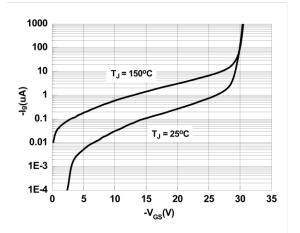


Figure 9. $I_g vs V_{GS}$

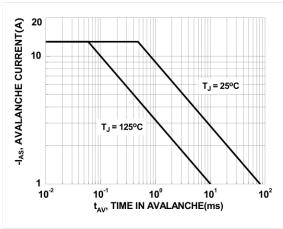


Figure 10. Unclamped Inductive Switching Capability

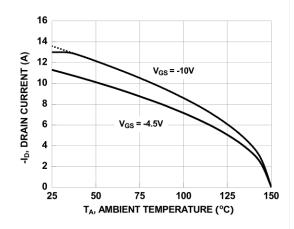


Figure 11. Maximum Continuous Drain Current vs
Ambient Temperature

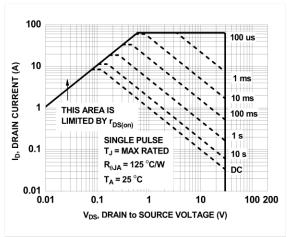


Figure 12. Forward Bias Safe Operating Area

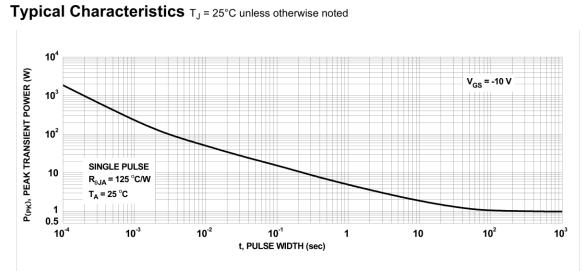


Figure 13. Single Pulse Maximum Power Dissipation

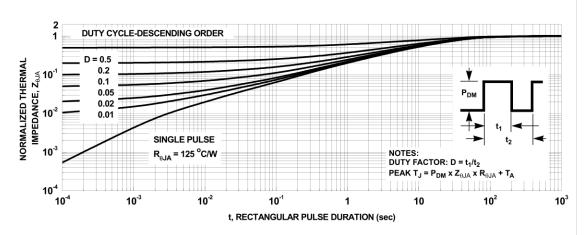


Figure 14. Junction-to-Ambient Transient Thermal Response Curve





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