International IR Rectifier

AUTOMOTIVE MOSFET

IRF1405

Typical Applications
- Electric Power Steering (EPS)
- Anti-lock Braking System (ABS)
- Wiper Control
- Climate Control
- Power Door

Benefits
- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax

Description
Specifically designed for Automotive applications, this Stripe Planar design of HEXFET® Power MOSFETs utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this HEXFET power MOSFET are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These benefits combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.

HEXFET® Power MOSFET

$V_{DSS} = 55V$

$R_{DS(on)} = 5.3m\Omega$

$I_D = 169A⑥$

TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	169⑥	
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	118⑥	A
I_{DM}	Pulsed Drain Current ①	680	
P_D @T_C = 25°C	Power Dissipation	330	W
	Linear Derating Factor	2.2	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	560	mJ
I_{AR}	Avalanche Current	See Fig.12a, 12b, 15, 16	A
E_{AR}	Repetitive Avalanche Energy⑦		mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J	Operating Junction and	-55 to + 175	
T_{STG}	Storage Temperature Range		°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	0.45	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	——	
$R_{\theta JA}$	Junction-to-Ambient	——	62	

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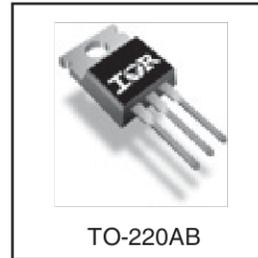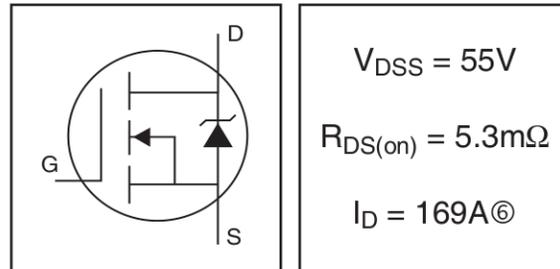
Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	——	——	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.057	——	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	4.6	5.3	mΩ	V_{GS} = 10V, I_D = 101A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0	V	V_{DS} = 10V, I_D = 250µA
g_{fs}	Forward Transconductance	69	——	——	S	V_{DS} = 25V, I_D = 110A
I_{DSS}	Drain-to-Source Leakage Current	——	——	20	µA	V_{DS} = 55V, V_{GS} = 0V
		——	——	250		V_{DS} = 44V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	200	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-200		V_{GS} = -20V
Q_g	Total Gate Charge	——	170	260		I_D = 101A
Q_{gs}	Gate-to-Source Charge	——	44	66	nC	V_{DS} = 44V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	62	93		V_{GS} = 10V④
$t_{d(on)}$	Turn-On Delay Time	——	13	——		V_{DD} = 38V
t_r	Rise Time	——	190	——	ns	I_D = 101A
$t_{d(off)}$	Turn-Off Delay Time	——	130	——		R_G = 1.1Ω
t_f	Fall Time	——	110	——		V_{GS} = 10V ④
L_D	Internal Drain Inductance	——	4.5	——	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	——	7.5	——		
C_{iss}	Input Capacitance	——	5480	——		V_{GS} = 0V
C_{oss}	Output Capacitance	——	1210	——	pF	V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	280	——		f = 1.0MHz, See Fig. 5
C_{oss}	Output Capacitance	——	5210	——		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	——	900	——		V_{GS} = 0V, V_{DS} = 44V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance ⑤	——	1500	——		V_{GS} = 0V, V_{DS} = 0V to 44V
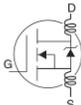
Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	169⑥	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	680		
V_{SD}	Diode Forward Voltage	——	——	1.3	V	T_J = 25°C, I_S = 101A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	——	88	130	ns	T_J = 25°C, I_F = 101A
Q_{rr}	Reverse RecoveryCharge	——	250	380	nC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).

② Starting T_J = 25°C, L = 0.11mH
   R_G = 25Ω, I_{AS} = 101A. (See Figure 12).

③ I_{SD} ≤ 101A, di/dt ≤ 210A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

④ Pulse width ≤ 400µs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.

⑦ Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.

2   www.irf.com

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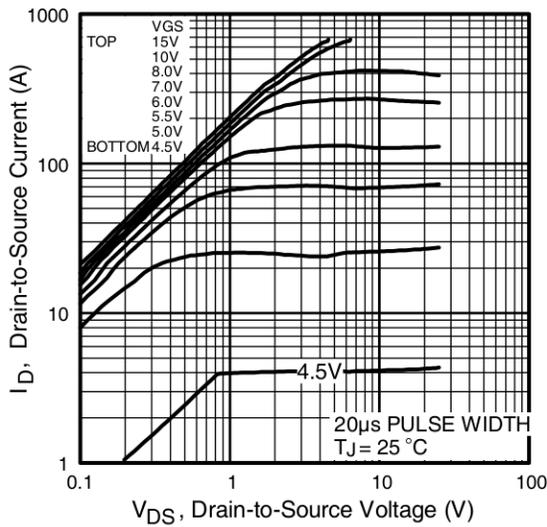
**Fig 1.** Typical Output Characteristics
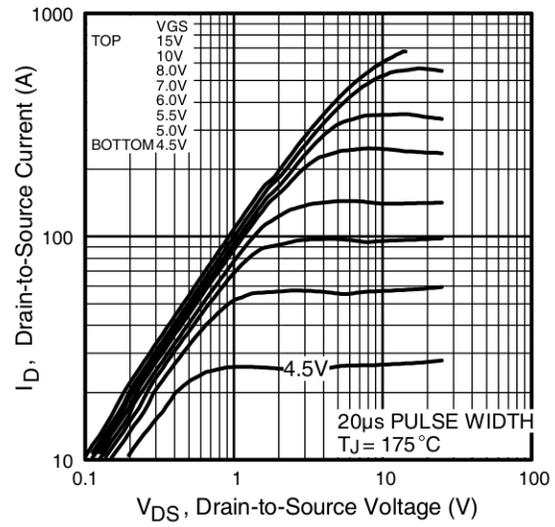
Fig 2. Typical Output Characteristics
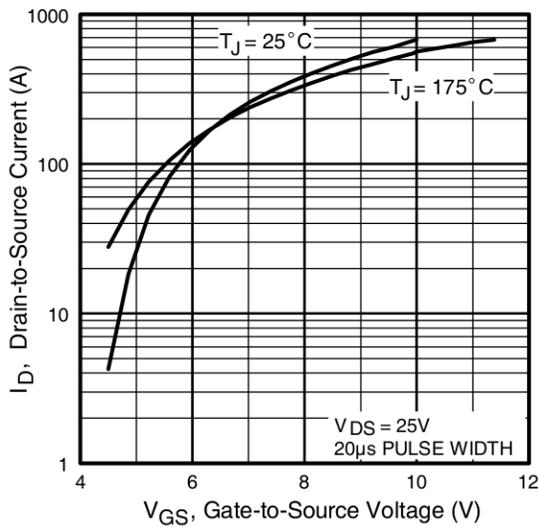
Fig 3. Typical Transfer Characteristics
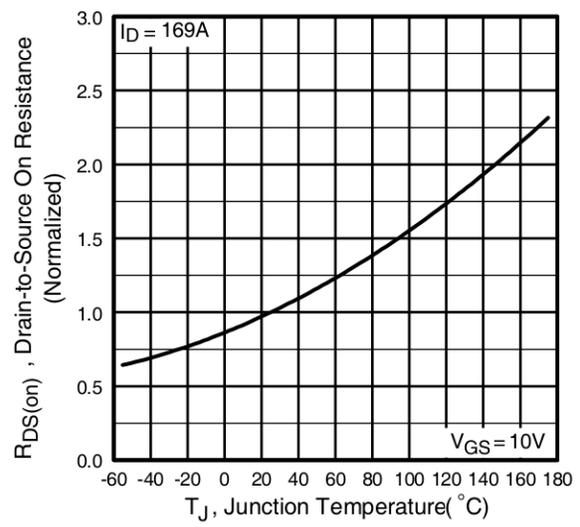
Fig 4. Normalized On-Resistance
Vs. Temperature

IRF1405

$V_{GS} = 0V, \quad f = 1\ MHZ$
$C_{iss} = C_{gs} + C_{gd}, \quad C_{ds} \quad SHORTED$
$C_{rss} = C_{gd}$
$C_{oss} = C_{ds} + C_{gd}$

Ciss
Coss
Crss

C, Capacitance(pF)

V_{DS}, Drain-to-Source Voltage (V)
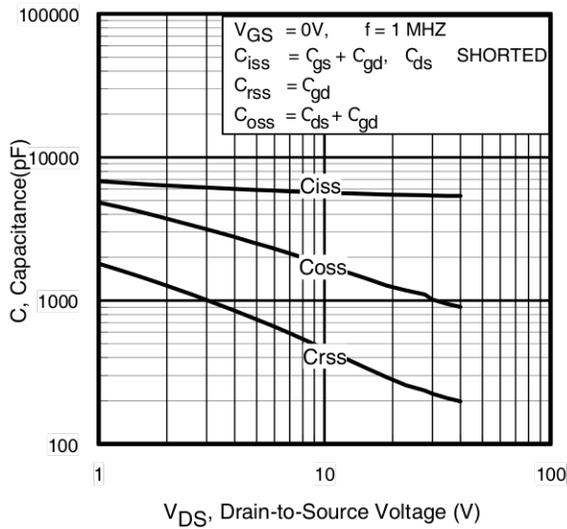
Fig 5. Typical Capacitance Vs.
Drain-to-Source Voltage

$I_D = 101A$

$V_{DS} = 44V$
$V_{DS} = 27V$

V_{GS}, Gate-to-Source Voltage (V)

FOR TEST CIRCUIT
SEE FIGURE 13

Q_G, Total Gate Charge (nC)
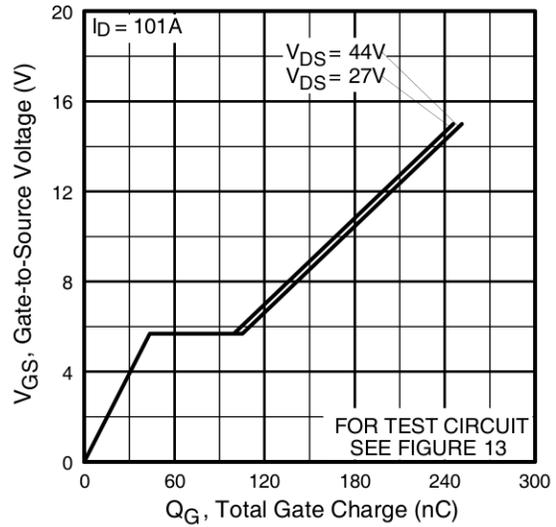
Fig 6. Typical Gate Charge Vs.
Gate-to-Source Voltage

$T_J = 175°C$

$T_J = 25°C$

$V_{GS} = 0\ V$

I_{SD}, Reverse Drain Current (A)

V_{SD}, Source-to-Drain Voltage (V)
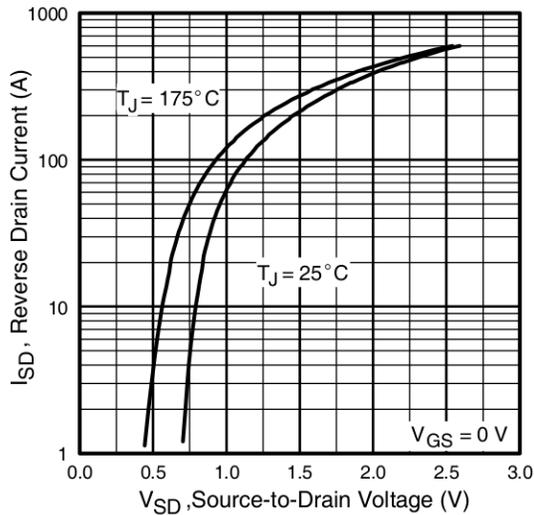
Fig 7. Typical Source-Drain Diode
Forward Voltage

OPERATION IN THIS AREA
LIMITED BY R_{DS}(on)

100μsec
1msec
10msec

Tc = 25°C
Tj = 175°C
Single Pulse

I_D, Drain-to-Source Current (A)

V_{DS}, Drain-toSource Voltage (V)
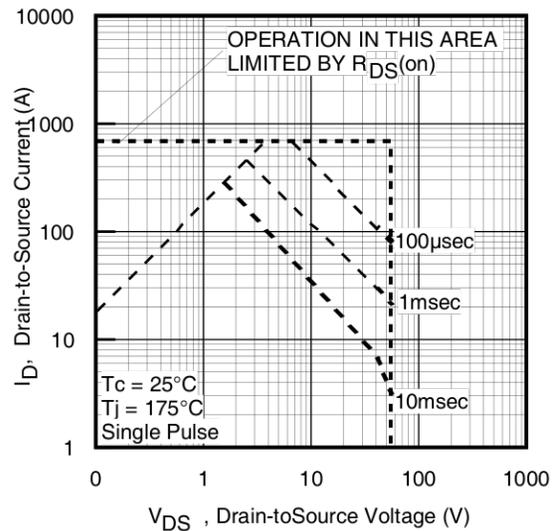
**Fig 8.** Maximum Safe Operating Area

4
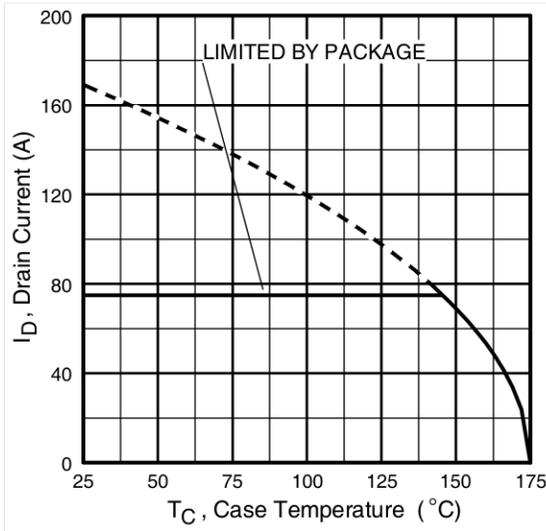
Fig 9. Maximum Drain Current Vs.
Case Temperature
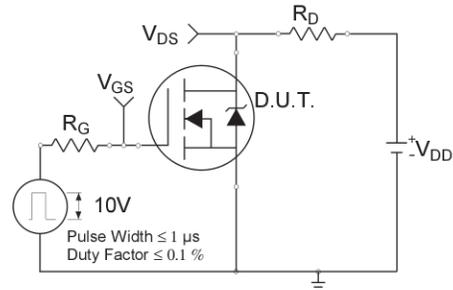
Fig 10a. Switching Time Test Circuit
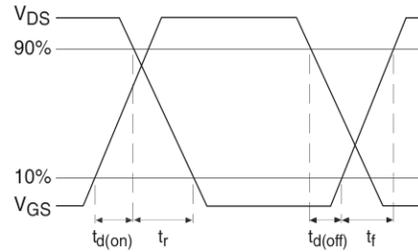
Fig 10b. Switching Time Waveforms

Notes:
1. Duty factor $D = t_1 / t_2$
2. Peak $T_J = P_{DM}$ x Z_{thJC} + T_C
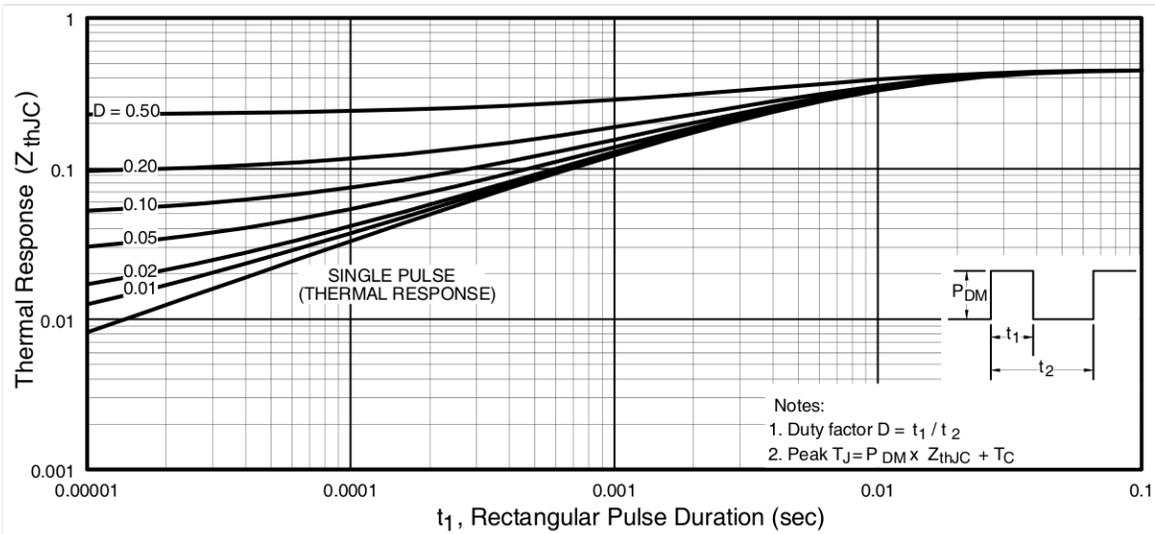
Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

IRF1405
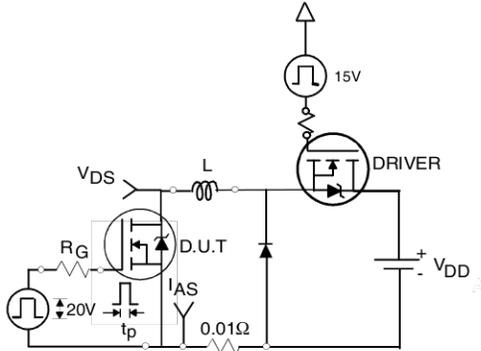
**Fig 12a.** Unclamped Inductive Test Circuit
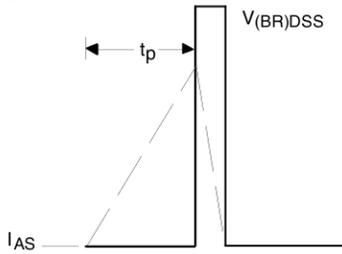
**Fig 12b.** Unclamped Inductive Waveforms
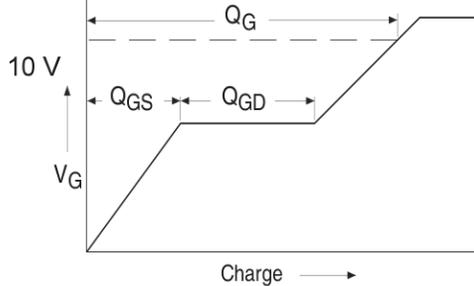
**Fig 13a.** Basic Gate Charge Waveform
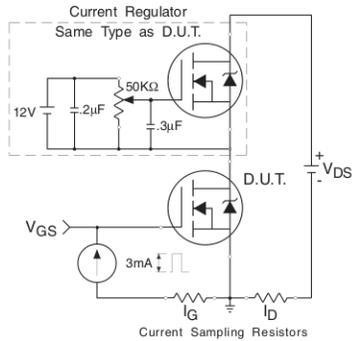
Fig 13b. Gate Charge Test Circuit
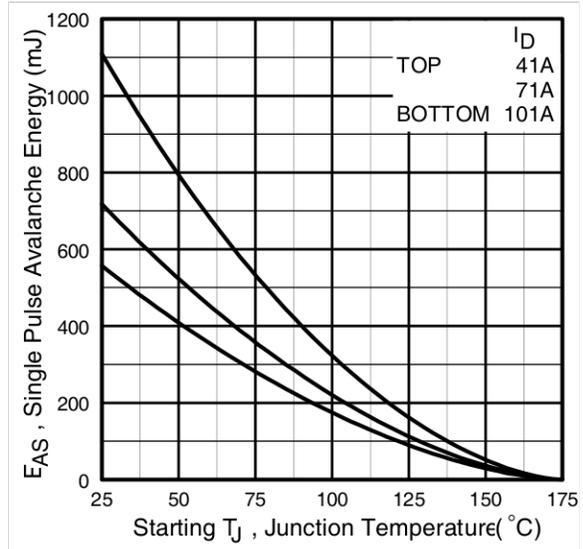

Fig 12c. Maximum Avalanche Energy
Vs. Drain Current
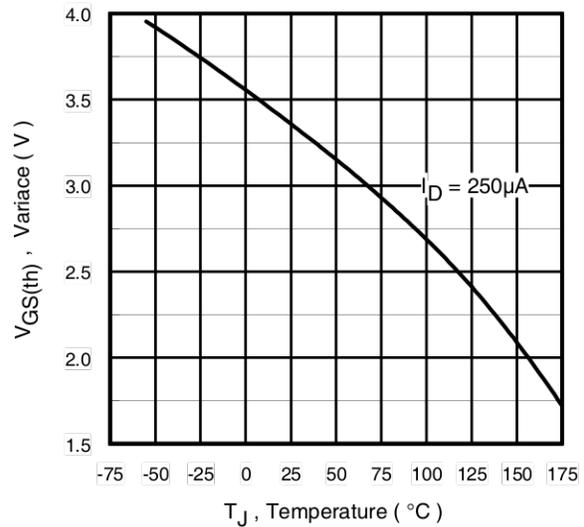
**Fig 14.** Threshold Voltage Vs. Temperature

6
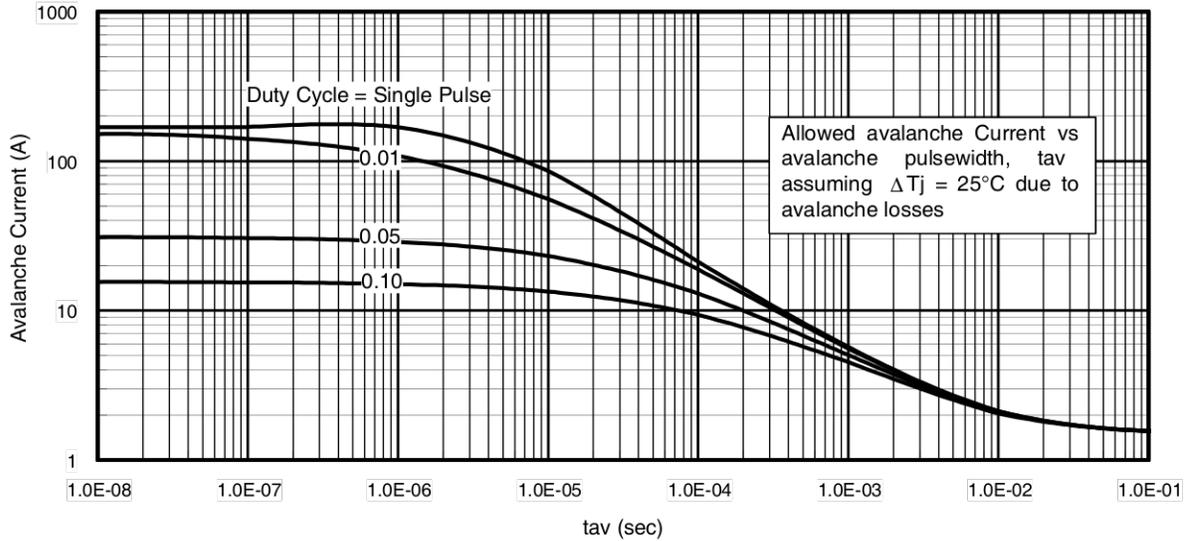
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**Fig 15.** Typical Avalanche Current Vs.Pulsewidth
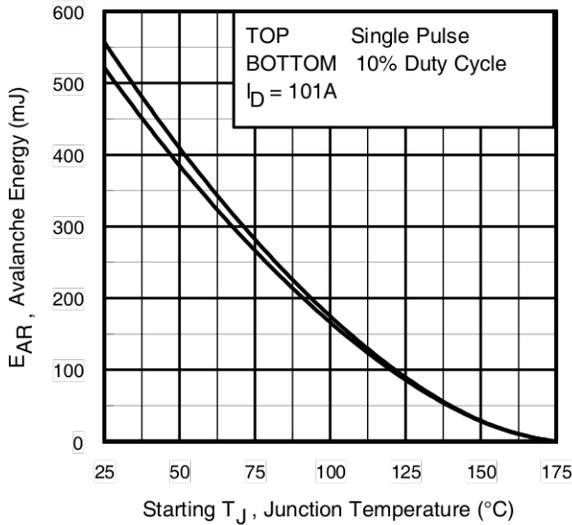
Fig 16. Maximum Avalanche Energy Vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
**(For further info, see AN-1005 at www.irf.com)**
1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D\ (ave)} = 1/2\ (\ 1.3 \cdot BV \cdot I_{av}) = \Delta T/\ Z_{thJC}$$
$$I_{av} = 2\Delta T/\ [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

Peak Diode Recovery dv/dt Test Circuit

D.U.T*

③

Circuit Layout Considerations
- Low Stray Inductance
- Ground Plane
- Low Leakage Inductance Current Transformer

+
②
-

④

①

R_G

- dv/dt controlled by R_G
- I_{SD} controlled by Duty Factor "D"
- D.U.T. - Device Under Test

+
- V_{DD}

V_{GS}
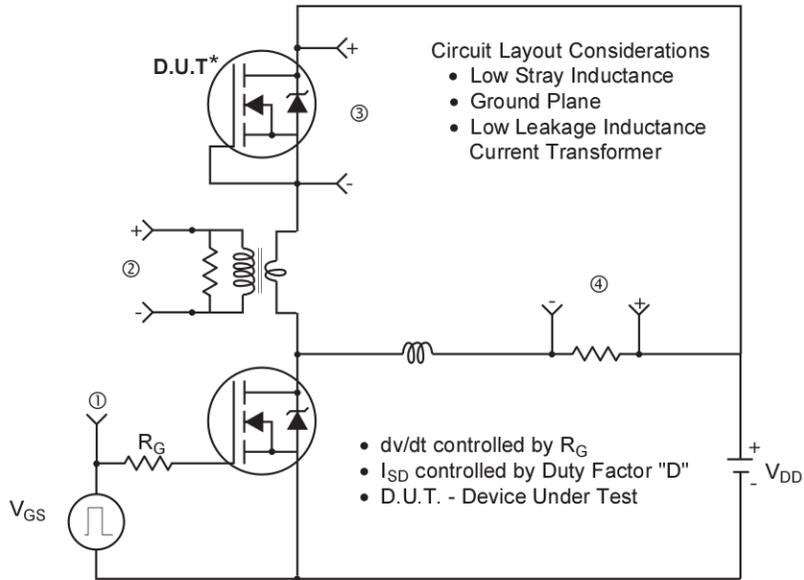
* Reverse Polarity of D.U.T for P-Channel

① Driver Gate Drive

$$D = \frac{P.W.}{Period}$$

P.W.

Period

$\left[V_{GS}=10V \right]$ ***

② D.U.T. I_{SD} Waveform

Reverse Recovery Current

Body Diode Forward Current

di/dt

③ D.U.T. V_{DS} Waveform

Diode Recovery dv/dt

$\left[V_{DD} \right]$

Re-Applied Voltage

Body Diode Forward Drop

④ Inductor Curent

$\left[I_{SD} \right]$

Ripple ≤ 5%
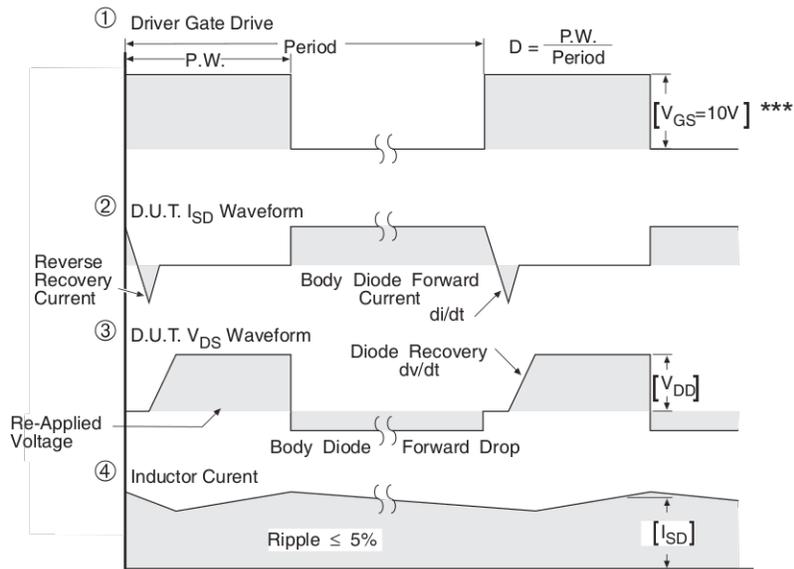
*** V_{GS} = 5.0V for Logic Level and 3V Drive Devices

Fig 17. For N-channel HEXFET® power MOSFETs

TO-220AB Package Outline (Dimensions are shown in millimeters (inches))
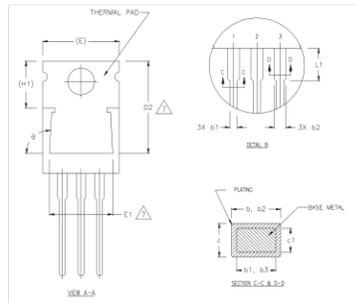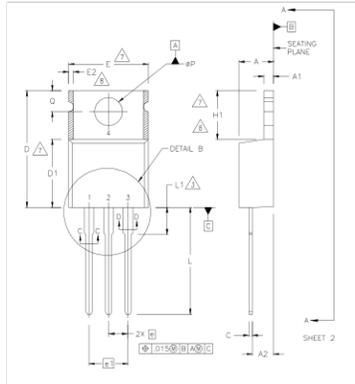
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5 M– 1994.
2. DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
3. LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. DIMENSION b1 & c1 APPLY TO BASE METAL ONLY.
6. CONTROLLING DIMENSION : INCHES.
7. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
8. DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.

LEAD ASSIGNMENTS

HEXFET
1.– GATE
2.– DRAIN
3.– SOURCE

IGBTs, CoPACK
1.– GATE
2.– COLLECTOR
3.– EMITTER

DIODES
1.– ANODE/OPEN
2.– CATHODE
3.– ANODE

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.82	.140	.190	
A1	0.51	1.40	.020	.055	
A2	2.04	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.96	.015	.038	5
b2	1.15	1.77	.045	.070	
b3	1.15	1.73	.045	.068	
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	12.19	12.88	.480	.507	7
E	9.66	10.66	.380	.420	4,7
E1	8.38	8.89	.330	.350	
e	2.54 BSC		.100 BSC		7
e1	5.08		.200 BSC		
H1	5.85	6.55	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	–	6.35	–	.250	3
øP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	
ø	90°–93°		90°–93°		

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead-Free"

INTERNATIONAL RECTIFIER LOGO

PART NUMBER

ASSEMBLY LOT CODE

DATE CODE
YEAR 7 = 1997
WEEK 19
LINE C

IRF1010
719C
17   89

TO-220AB packages are not recommended for Surface Mount Application.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Automotive [Q101] market.
Qualification Standards can be found on IR's Web site.

International IƎR Rectifier

Note: For the most current drawings please refer to the IR website at:
http://www.irf.com/package/