Data Sheet No. PD60253

International
IOR Rectifier

# IRS2111(S)PbF

## HALF-BRIDGE DRIVER

### Features

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for both channels
- CMOS Schmitt-triggered inputs with pull-down
- Matched propagation delay for both channels
- Internally set deadtime
- High-side output in phase with input
- RoHS compliant

### Product Summary

| | |
|---|---|
| $V_{OFFSET}$ | 600 V max. |
| $I_{O}$+/- | 200 mA / 420 mA |
| $V_{OUT}$ | 10 V - 20 V |
| $t_{on/off}$ (typ.) | 750 ns & 150 ns |
| Deadtime (typ.) | 650 ns |

### Description

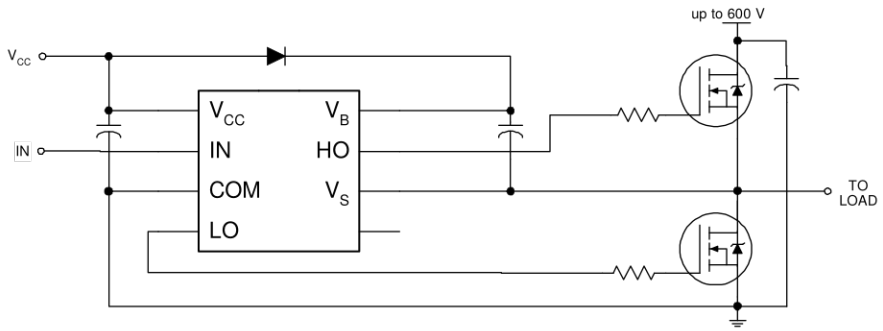
The IRS2111 is a high voltage, high speed power MOSFET and IGBT driver with dependent high-side and low-side referenced output channels designed for half-bridge applications. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic input is compatible with standard CMOS outputs. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Internal deadtime is provided to avoid shoot-through in the output half-bridge. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600 V.

### Packages

8-Lead PDIP
IRS2111PbF

8-Lead SOIC
IRS21111SPbF

### Typical Connection




(Refer to Lead Assignments for correct pin configuration). This diagram shows electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

## Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Additional information is shown in Figs. 7 through 10.

| Symbol | Definition | | Min. | Max. | Units |
|---|---|---|---|---|---|
| $V_B$ | High-side floating supply voltage | | -0.3 | 625 (Note 1) | V |
| $V_S$ | High-side floating supply offset voltage | | $V_B$ - 25 | $V_B$ + 0.3 | |
| $V_{HO}$ | High-side floating output voltage | | $V_S$ - 0.3 | $V_B$ + 0.3 | |
| $V_{CC}$ | Low-side and logic fixed supply voltage | | -0.3 | 25 (Note 1) | |
| $V_{LO}$ | Low-side output voltage | | -0.3 | $V_{CC}$ + 0.3 | |
| $V_{IN}$ | Logic input voltage | | -0.3 | $V_{CC}$ + 0.3 | |
| $dV_S/dt$ | Allowable offset supply voltage transient (Fig. 2) | | — | 50 | V/ns |
| $P_D$ | Package power dissipation @ $T_A \leq +25$ °C | (8 Lead PDIP) | — | 1.0 | W |
| | | (8 lead SOIC) | — | 0.625 | |
| $Rth_{JA}$ | Thermal resistance, junction to ambient | (8 lead PDIP) | — | 125 | °C/W |
| | | (8 lead SOIC) | — | 200 | |
| $T_J$ | Junction temperature | | — | 150 | °C |
| $T_S$ | Storage temperature | | -55 | 150 | |
| $T_L$ | Lead temperature (soldering, 10 seconds) | | — | 300 | |

Note 1: All supplies are fully tested at 25 V, and an internal 20 V clamp exists for each supply

## Recommended Operating Conditions

The input/output logic timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. The $V_S$ offset rating is tested with all supplies biased at a 15 V differential.

| Symbol | Definition | Min. | Max. | Units |
|---|---|---|---|---|
| $V_B$ | High-side floating supply absolute voltage | $V_S$ + 10 | $V_S$ + 20 | V |
| $V_S$ | High-side floating supply offset voltage | Note 2 | 600 | |
| $V_{HO}$ | High-side floating output voltage | $V_S$ | $V_B$ | |
| $V_{CC}$ | Low-side and logic fixed supply voltage | 10 | 20 | |
| $V_{LO}$ | Low-side output voltage | 0 | $V_{CC}$ | |
| $V_{IN}$ | Logic input voltage | 0 | $V_{CC}$ | |
| $T_A$ | Ambient temperature | -40 | 125 | °C |

Note 2: Logic operational for $V_S$ of -5 V to +600 V. Logic state held for $V_S$ of -5 V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).

## Dynamic Electrical Characteristics

$V_{BIAS}$ ($V_{CC}$, $V_{BS}$) = 15 V, $C_L$ = 1000 pF and $T_A$ = 25 °C unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Fig. 3.

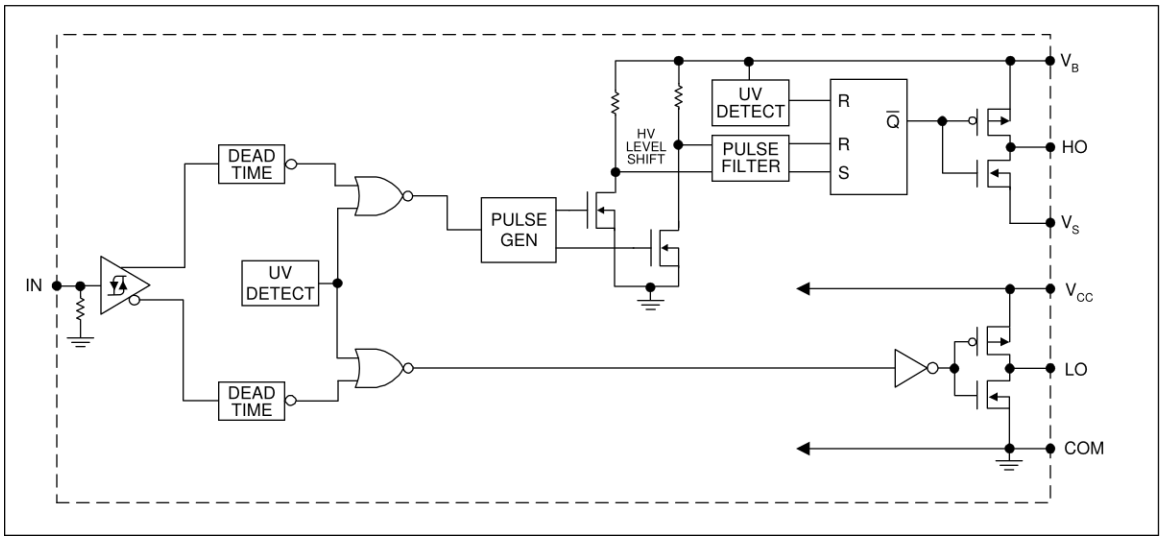
| Symbol | Definition | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $t_{on}$ | Turn-on propagation delay | 550 | 750 | 950 | ns | $V_S$ = 0 V |
| $t_{off}$ | Turn-off propagation delay | — | 150 | 180 | | $V_S$ = 600 V |
| $t_r$ | Turn-on rise time | — | 75 | 130 | | |
| $t_f$ | Turn-off fall time | — | 35 | 65 | | |
| DT | Deadtime, LS turn-off to HS turn-on & HS turn-off to LS turn-on | 480 | 650 | 820 | | |
| MT | Delay matching, HS & LS turn-on/off | — | 30 | — | | |

## Static Electrical Characteristics

$V_{BIAS}$ ($V_{CC}$, $V_{BS}$) = 15 V and $T_A$ = 25 °C unless otherwise specified. The $V_{IN}$, $V_{TH}$, and $I_{IN}$ parameters are referenced to COM. The $V_O$ and $I_O$ parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

| Symbol | Definition | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Logic “1” input voltage for HO & logic “0” for LO | 6.4 | — | — | V | $V_{CC}$ = 10 V |
| | | 9.5 | — | — | | $V_{CC}$ = 15 V |
| | | 12.6 | — | — | | $V_{CC}$ = 20 V |
| $V_{IL}$ | Logic “0” input voltage for HO & logic “1” for LO | — | — | 3.8 | | $V_{CC}$ = 10 V |
| | | — | — | 6.0 | | $V_{CC}$ = 15 V |
| | | — | — | 8.3 | | $V_{CC}$ = 20 V |
| $V_{OH}$ | High level output voltage, $V_{BIAS}$ - $V_O$ | — | 0.05 | 0.2 | | $I_O$ = 2 mA |
| $V_{OL}$ | Low level output voltage, $V_O$ | — | 0.02 | 0.1 | | |
| $I_{LK}$ | Offset supply leakage current | — | — | 50 | µA | $V_B$ = $V_S$ = 600 V |
| $I_{QBS}$ | Quiescent $V_{BS}$ supply current | — | 50 | 100 | | $V_{IN}$ = 0 V or $V_{CC}$ |
| $I_{QCC}$ | Quiescent $V_{CC}$ supply current | — | 70 | 180 | | |
| $I_{IN+}$ | Logic “1” input bias current | — | 30 | 50 | | $V_{IN}$ = $V_{CC}$ |
| $I_{IN-}$ | Logic “0” input bias current | — | — | 5.0 | | $V_{IN}$ = 0 V |
| $V_{BSUV+}$ | $V_{BS}$ supply undervoltage positive going threshold | 7.6 | 8.6 | 9.6 | V | |
| $V_{BSUV-}$ | $V_{BS}$ supply undervoltage negative going threshold | 7.2 | 8.2 | 9.2 | | |
| $V_{CCUV+}$ | $V_{CC}$ supply undervoltage positive going threshold | 7.6 | 8.6 | 9.6 | | |
| $V_{CCUV-}$ | $V_{CC}$ supply undervoltage negative going threshold | 7.2 | 8.2 | 9.2 | | |
| $I_{O+}$ | Output high short circuit pulsed current | 200 | 290 | — | mA | $V_O$ = 0 V, $V_{IN}$ = $V_{CC}$ PW ≤10 µs |
| $I_{O-}$ | Output low short circuit pulsed current | 420 | 600 | — | | $V_O$ = 15 V, $V_{IN}$ = 0 V PW ≤10 µs |

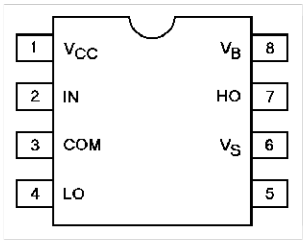
## Functional Block Diagram



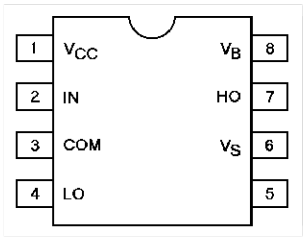

## Lead Definitions

| Symbol | Description |
|---|---|
| IN | Logic input for high-side and low-side gate driver outputs (HO & LO), in phase with HO |
| $V_B$ | High-side floating supply |
| HO | High-side gate drive output |
| $V_S$ | High-side floating supply return |
| $V_{CC}$ | Low-side and logic fixed supply |
| LO | Low-side gate drive output |
| COM | Low-side return |

## Lead Assignments




8 Lead DIP




8 Lead SOIC

| IRS2111 | IRS2111S |
|---|---|
| Part Number | |

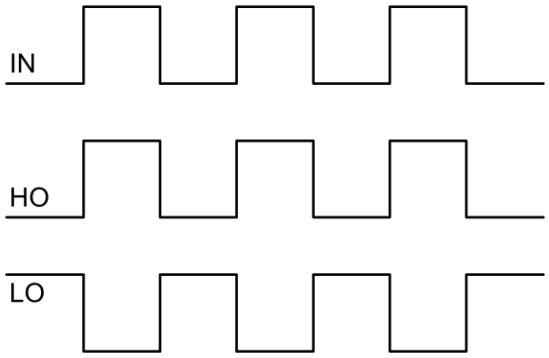



Figure 1. Input/Output Timing Diagram

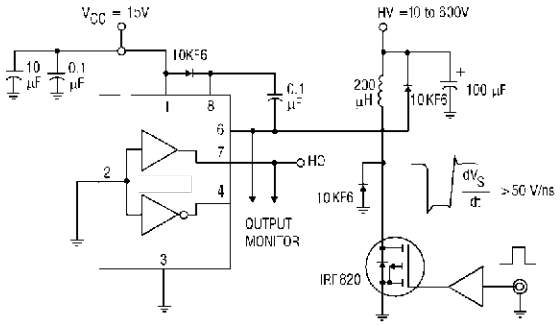



Figure 2. Floating Supply Voltage Transient Test Circuit

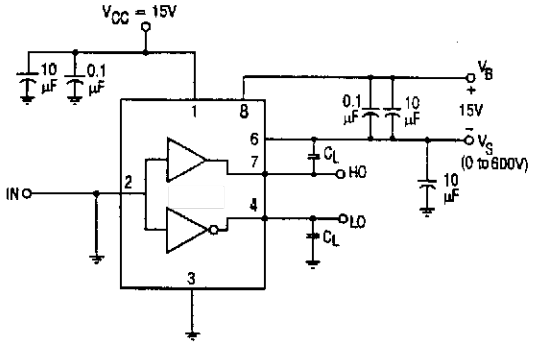



Figure 3. Switching Time Test Circuit

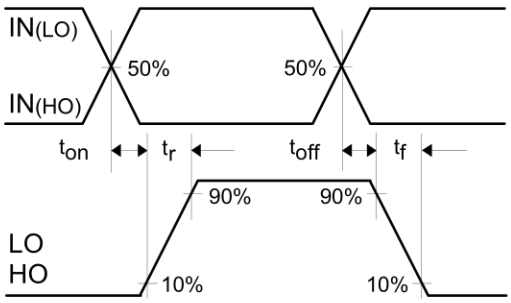



Figure 4. Switching Time Waveform Definition

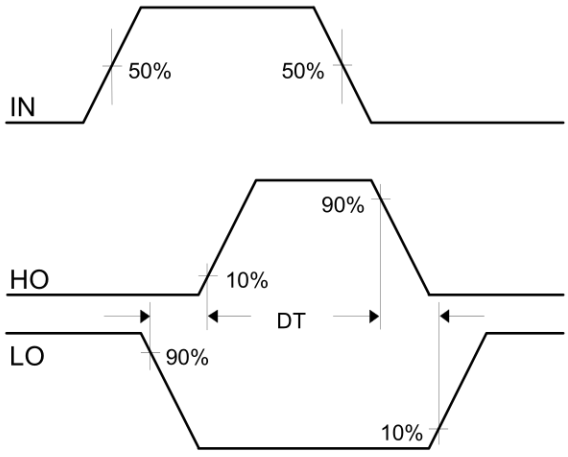



Figure 5. Deadtime Waveform Definitions

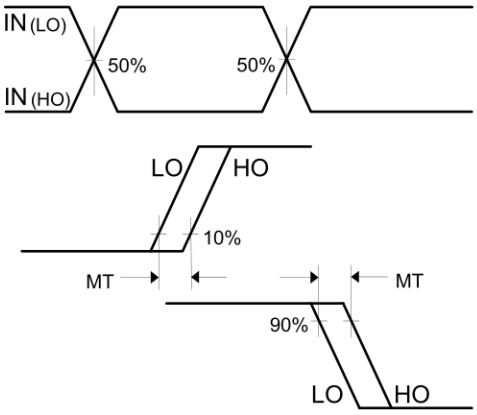



Figure 6. Delay Matching Waveform Definitions

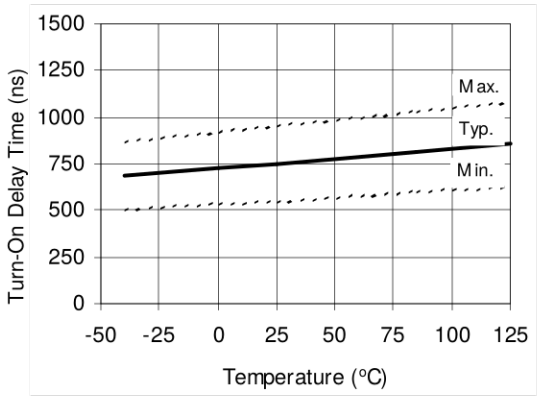



**Figure 7A Turn-On Time vs Temperature**

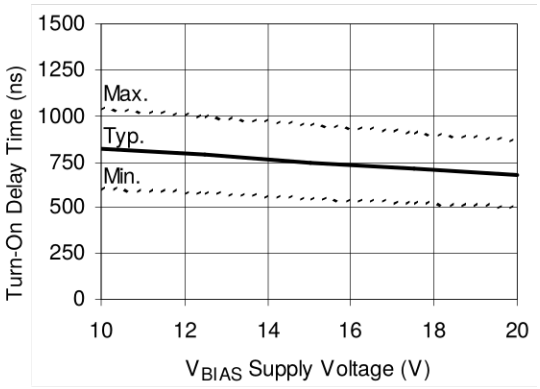



**Figure 7B Turn-On Time vs Voltage**

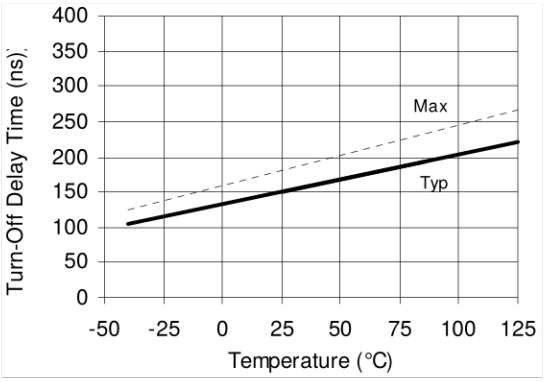



**Figure 8A Turn-Off Time vs Temperature**

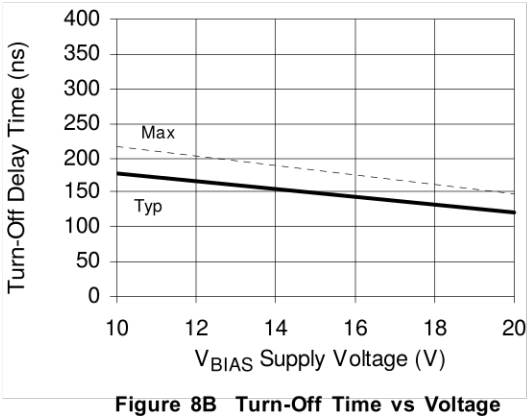



**Figure 8B Turn-Off Time vs Voltage**

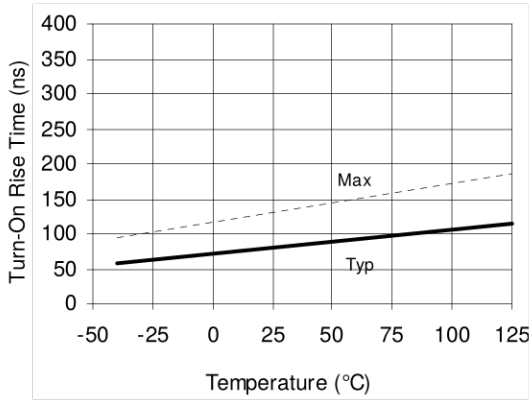



**Figure 9A Turn-On Rise Time vs Temperature**

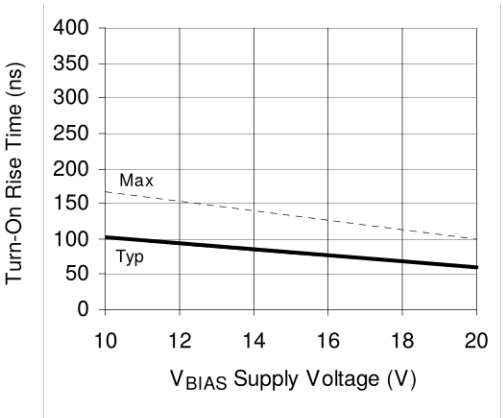



**Figure 9B Turn-On Rise Time vs Voltage**

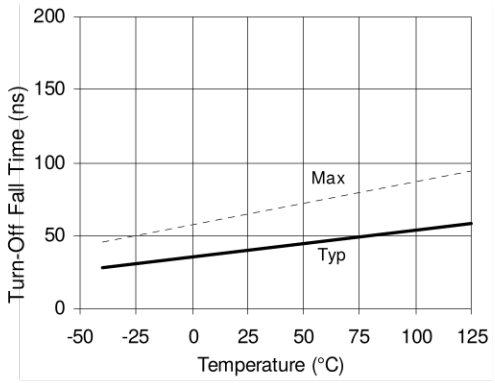



**Figure 10A Turn-Off Fall Time vs Temperature**

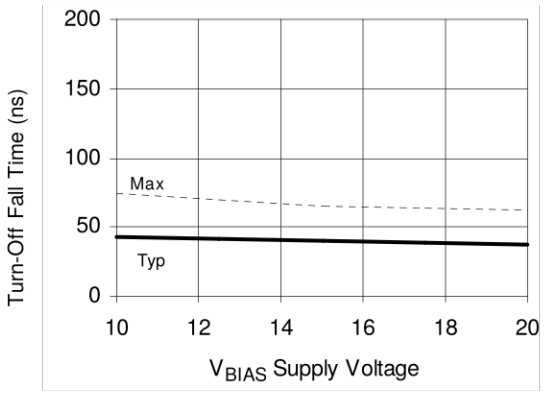



**Figure 10B Turn-Off Fall Time vs Voltage**

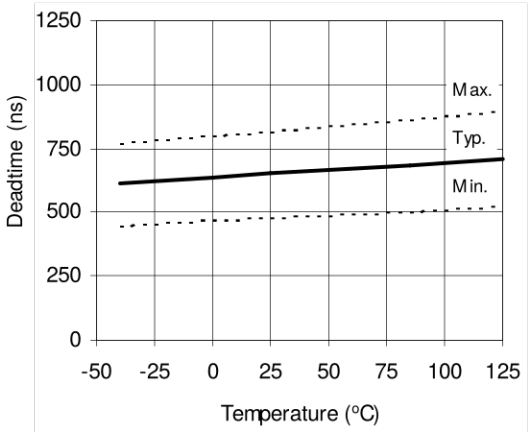



**Figure 11A Deadtime vs Temperature**

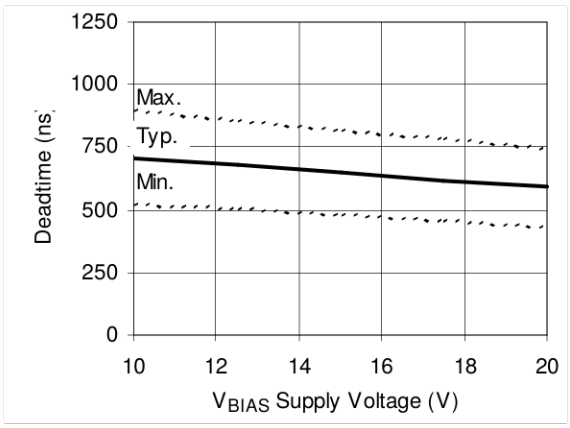



**Figure 11B Deadtime vs Voltage**

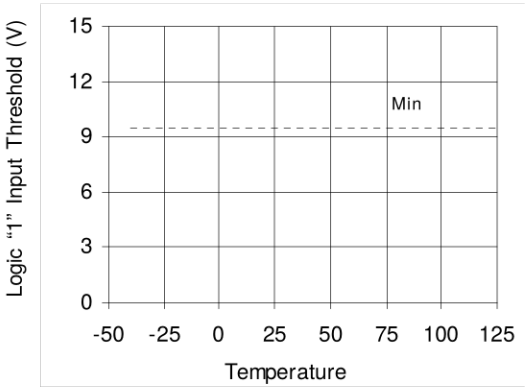



**Figure 12A Logic "I" Input voltage for HO & Logic "0" for LO vs Temperature**

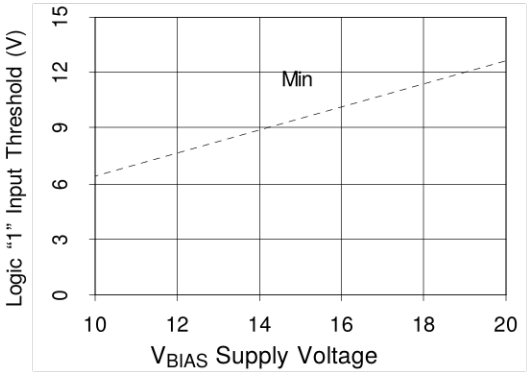



**Figure 12B Logic "I" Input voltage for HO & Logic "0" for LO vs Voltage**

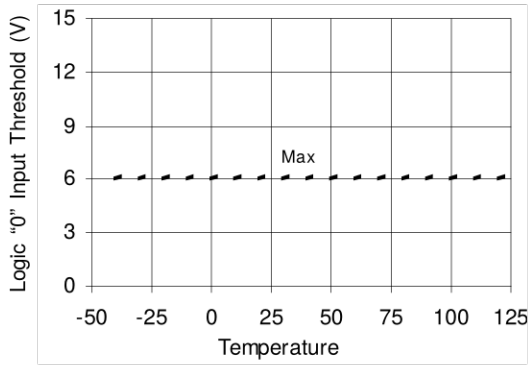



**Figure 13A Logic "0" Input voltage for HO & Logic "I" for LO vs Temperature**

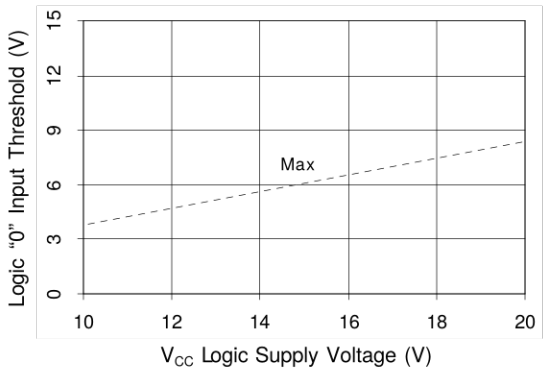



**Figure 13B Logic "0" Input voltage for HO & Logic "I" for LO vs Voltage**

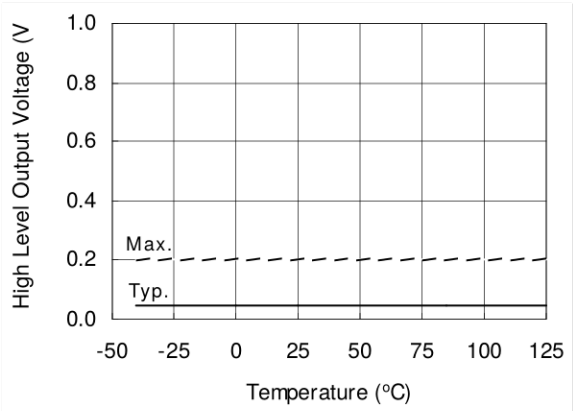



**Figure 14A. High Level Output vs. Temperature**

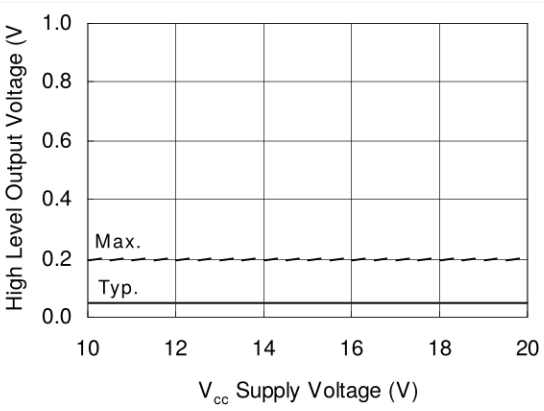



**Figure 14B. High Level Output vs. Supply Voltage**

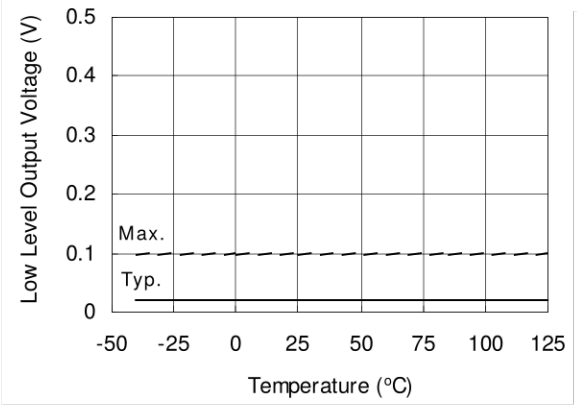



**Figure 15A. Low Level Output vs. Temperature**

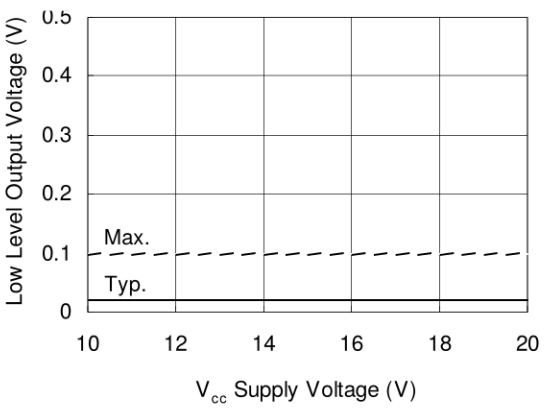



**Figure 15B. Low Level Output vs. Voltage**

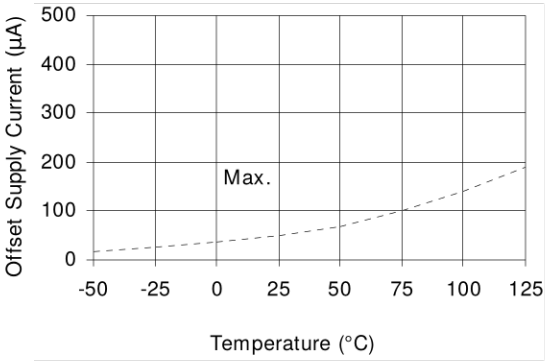



**Figure 16A Offset Supply Current vs Temperature**

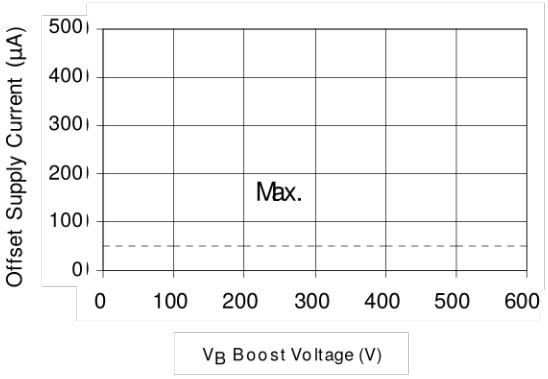



**Figure 16B Offset Supply Current vs Voltage**

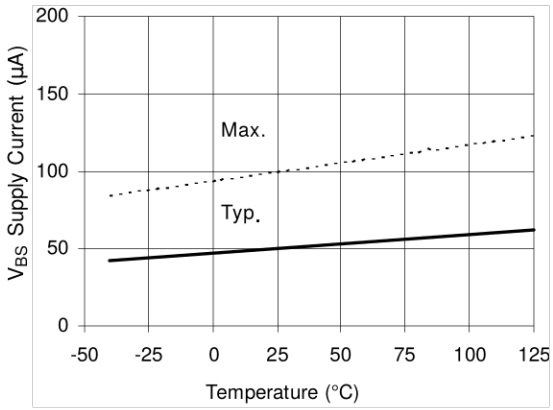



**Figure 17A $V_{BS}$ Supply Current vs Temperature**

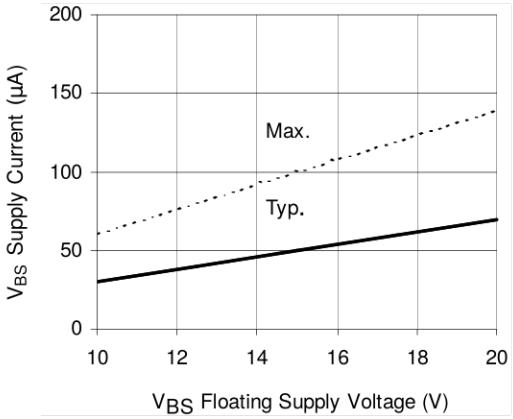



**Figure 17B $V_{BS}$ Supply Current vs Voltage**

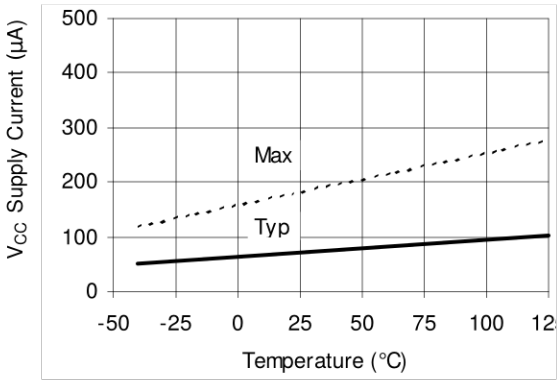



**Figure 18A $V_{CC}$ Supply Current vs Temperature**

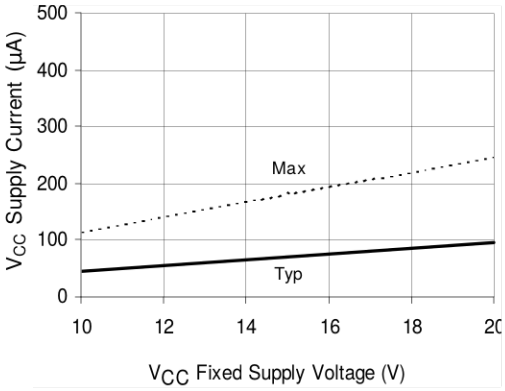



**Figure 18B $V_{CC}$ Supply Current vs Voltage**

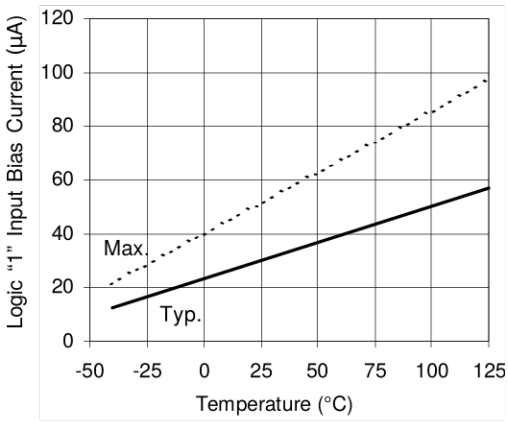



**Figure 19A Logic "1" Input Current vs. Temperature**

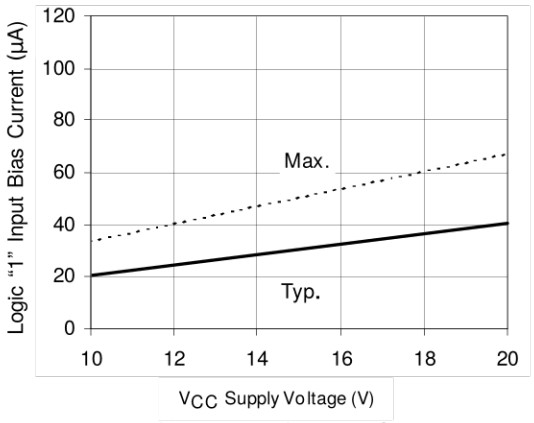



**Figure 19B Logic "1" Input Current vs. $V_{CC}$ Voltage**

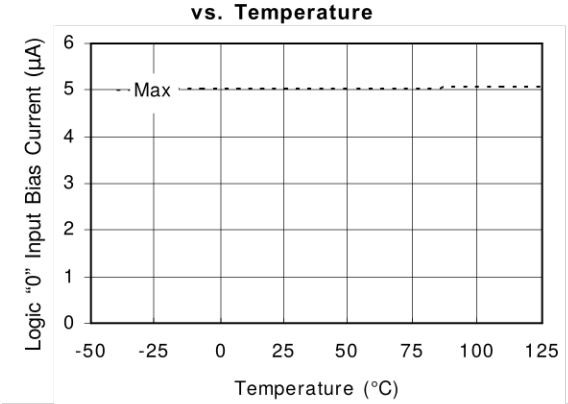



**Figure 20A. Logic "0" Input Bias Current vs. Temperature**

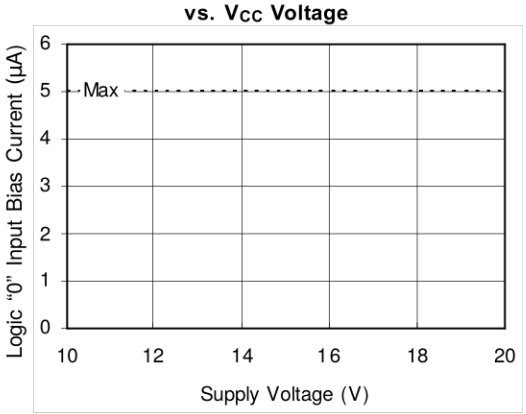



**Figure 20B. Logic "0" Input Bias Current vs. $V_{CC}$ Voltage**

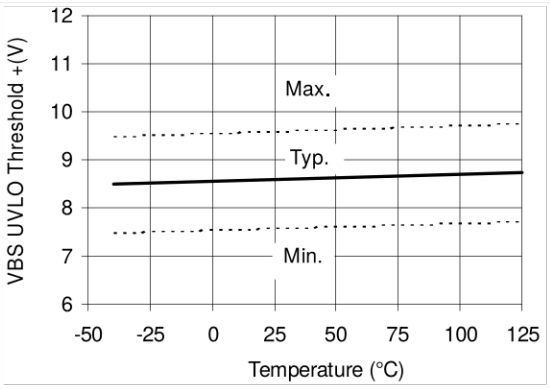



**Figure 21 $V_{BS}$ Undervoltage Threshold (+) vs. Temperature**

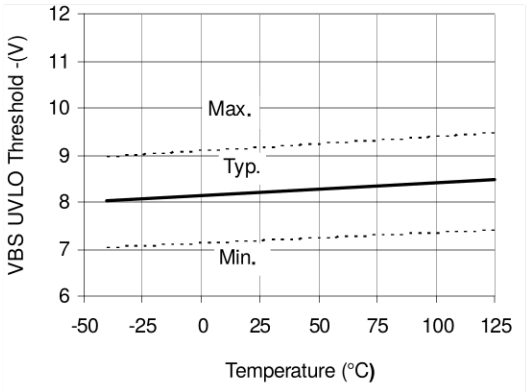



**Figure 22 $V_{BS}$ Undervoltage Threshold (-) vs. Temperature**

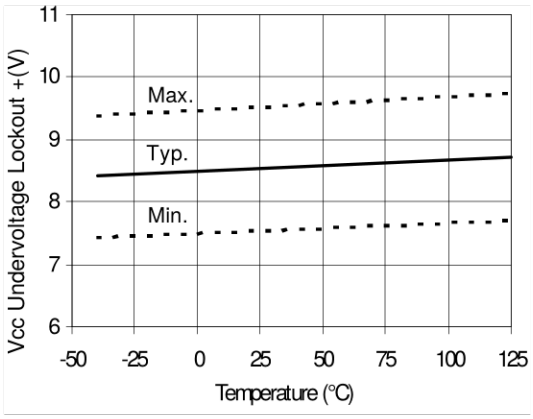



**Figure 23 $V_{CC}$ Undervoltage (-) vs Temperature**

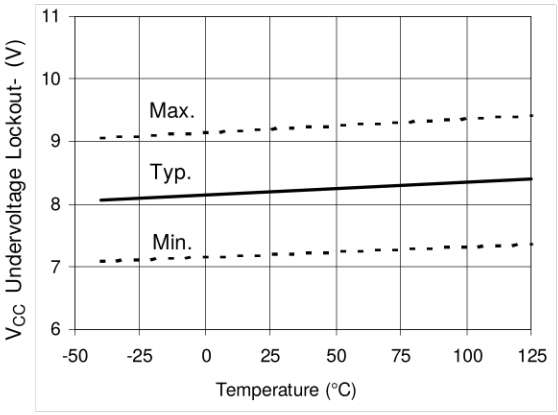



**Figure 24 $V_{CC}$ Undervoltage (-) vs Temperature**

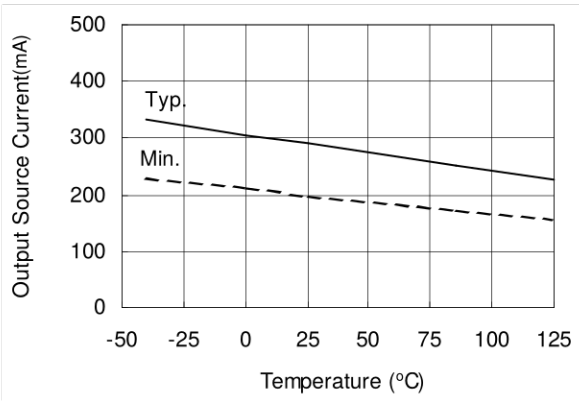



**Figure 25A Output Source Current vs Temperature**

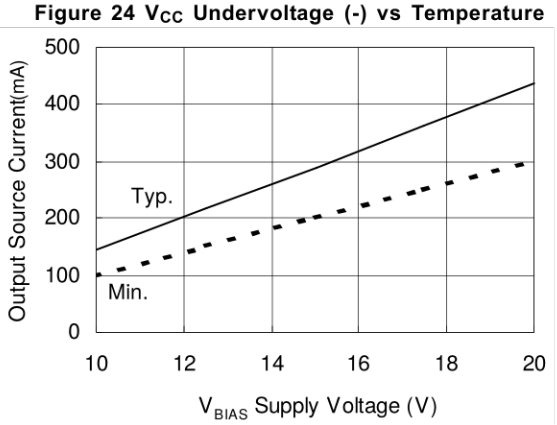



**Figure 25B Output Source Current vs Voltage**

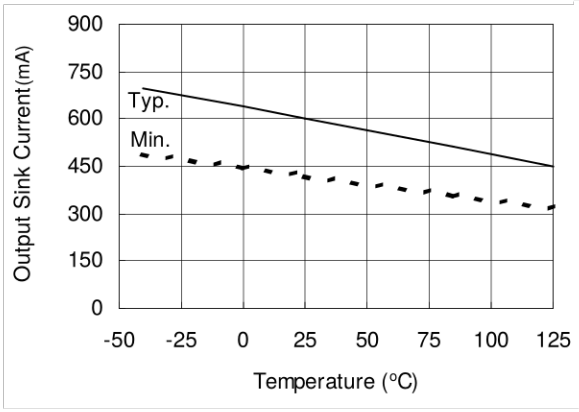



**Figure 26A Output Sink Current vs Temperature**

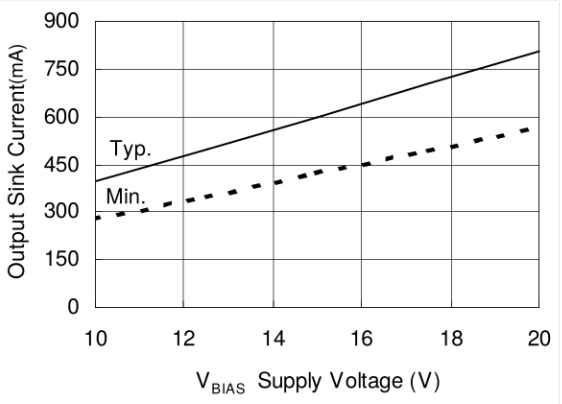



**Figure 26B Output Sink Current vs Voltage**

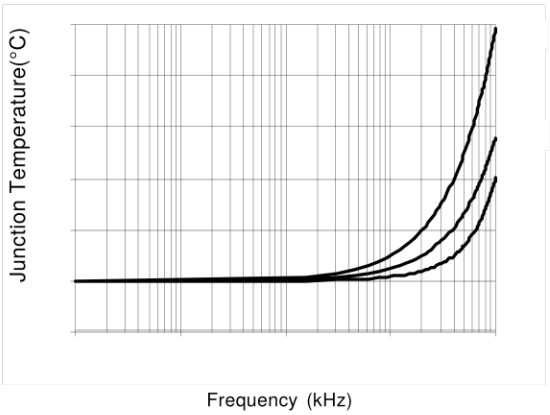



**Figure 27. IRS2111 TJ vs. Frequency (IRFBC20)**
**$R_{GATE}$ = 33 Ω, $V_{CC}$ = 15 V**

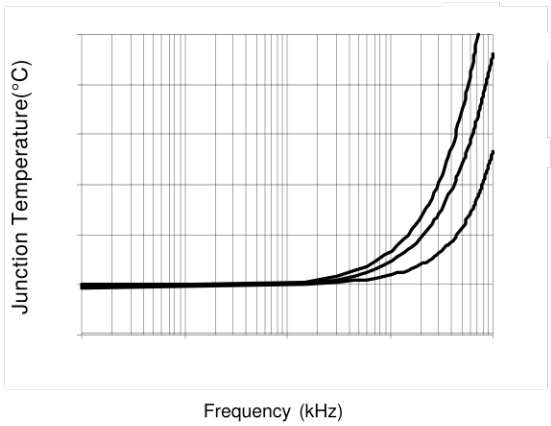



**Figure 28. IRS2111 TJ vs. Frequency (IRFBC30)**
**$R_{GATE}$ = 22 Ω, $V_{CC}$ = 15 V**

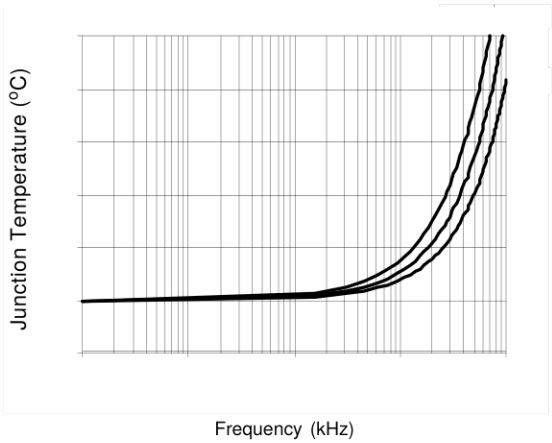



**Figure 29. IRS2111 TJ vs. Frequency (IRFBC40)**
**$R_{GATE}$ = 15 Ω, $V_{CC}$ = 15 V**

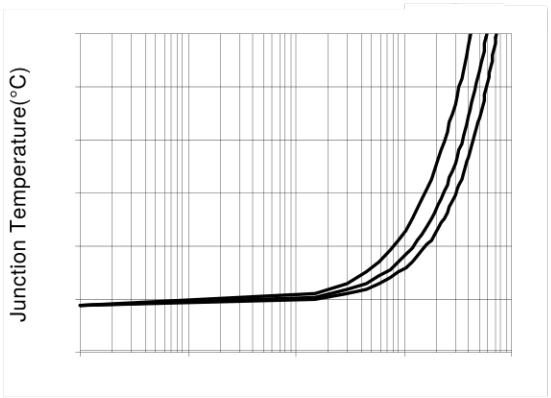



**Figure 30. IRS2111 TJ vs. Frequency (IRFPC50)**
**$R_{GATE}$ = 10 Ω, $V_{CC}$ = 15 V**

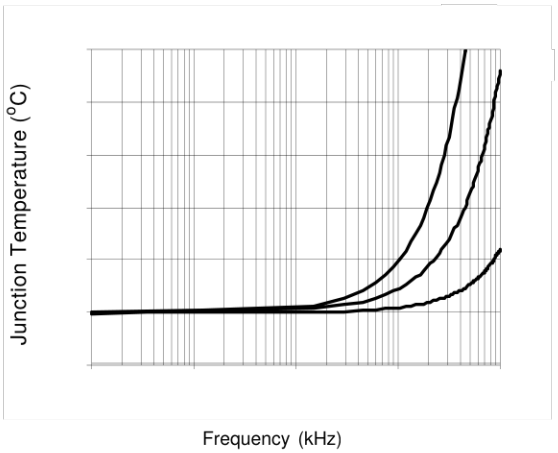



**Figure 31. IRS2111S TJ vs. Frequency (IRFBC20)**
**$R_{GATE}$ = 33 Ω, $V_{CC}$ = 15 V**

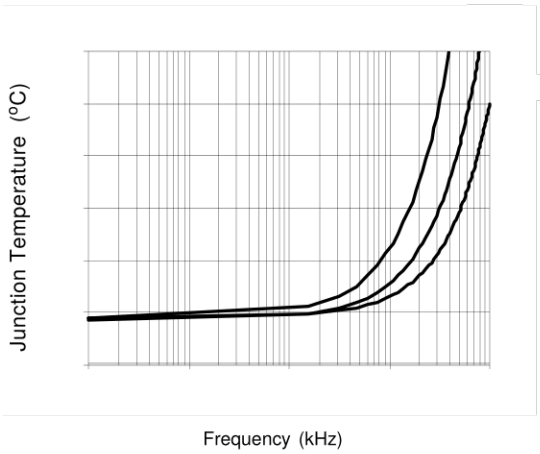



**Figure 32. IRS2111S TJ vs. Frequency (IRFBC30)**
**$R_{GATE}$ = 22 Ω, $V_{CC}$ = 15 V**

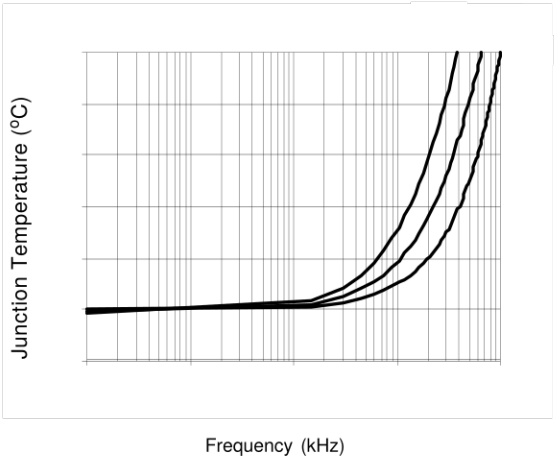



**Figure 33. IRS2111S TJ vs. Frequency (IRFBC40)**
**$R_{GATE}$ = 15 Ω, $V_{CC}$ = 15 V**

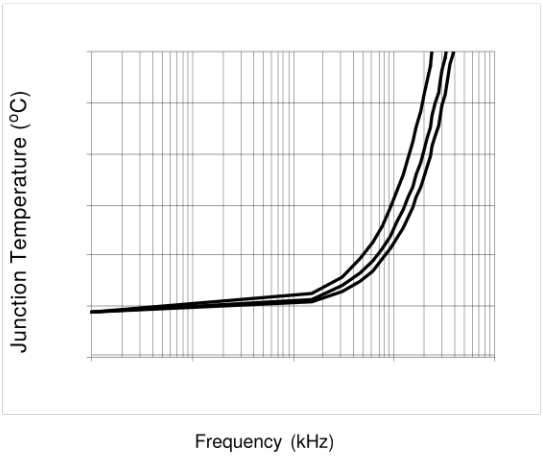
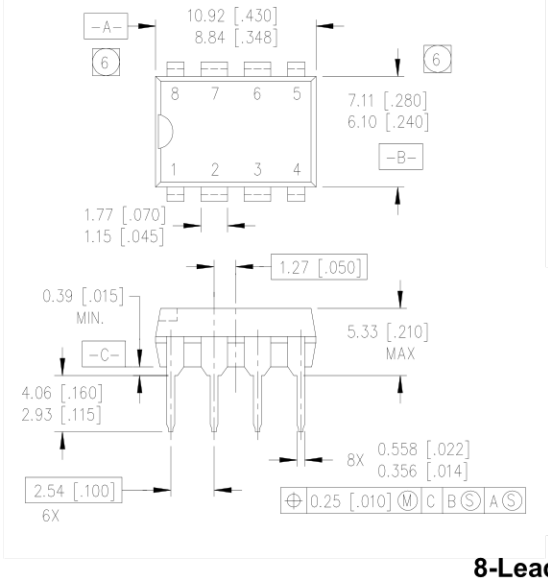



**Figure 34. IRS2111S TJ vs. Frequency (IRFPC50)**
**$R_{GATE}$ = 10 Ω, $V_{CC}$ = 15 V**

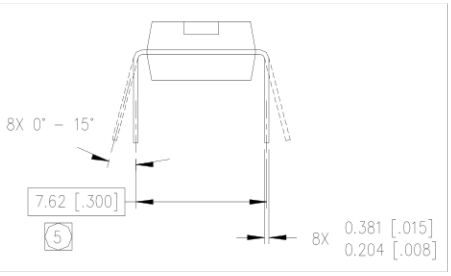
## Case outlines




NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M–1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS–001AB.

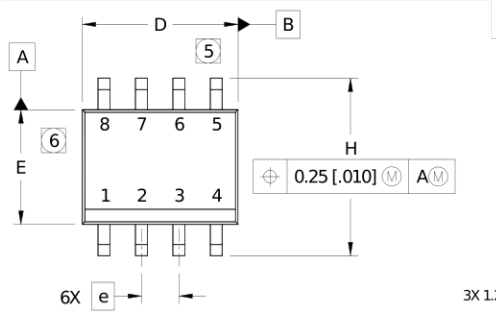
(5) MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.

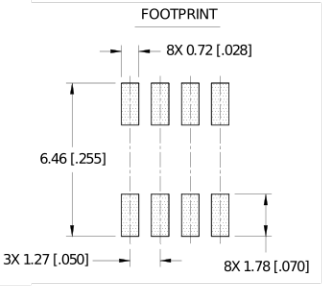
(6) DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



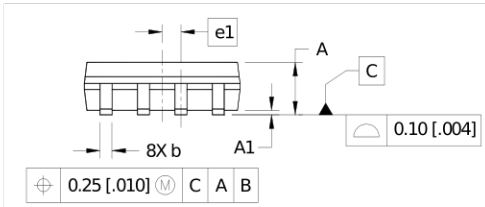

**8-Lead PDIP**

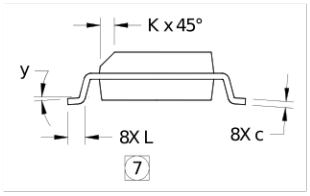
01-6014
01-3003 01 (MS-001AB)




| DIM | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | .0532 | .0688 | 1.35 | 1.75 |
| A1 | .0040 | .0098 | 0.10 | 0.25 |
| b | .013 | .020 | 0.33 | 0.51 |
| c | .0075 | .0098 | 0.19 | 0.25 |
| D | .189 | .1968 | 4.80 | 5.00 |
| E | .1497 | .1574 | 3.80 | 4.00 |
| e | .050 BASIC | | 1.27 BASIC | |
| e 1 | .025 BASIC | | 0.635 BASIC | |
| H | .2284 | .2440 | 5.80 | 6.20 |
| K | .0099 | .0196 | 0.25 | 0.50 |
| L | .016 | .050 | 0.40 | 1.27 |
| y | 0° | 8° | 0° | 8° |




NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO J EDEC OUTLINE MS-012AA.

(5) DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].

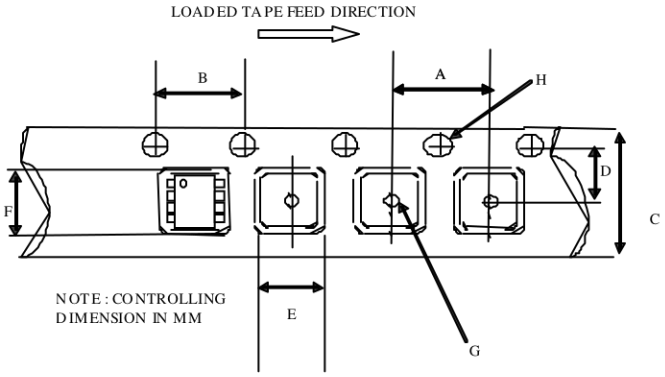
(6) DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].

(7) DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

**8-Lead SOIC**

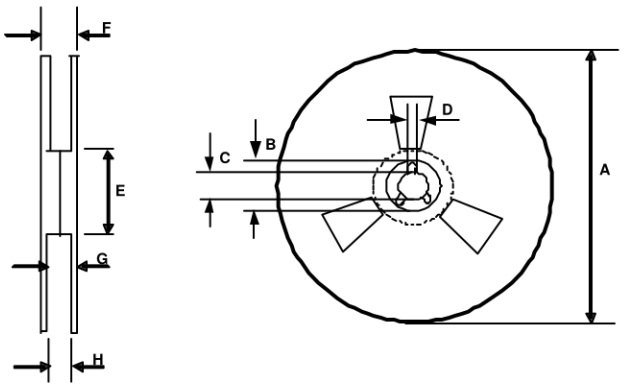
01-6027
01-0021 11 (MS-012AA)

## Tape & Reel
## 8-lead SOIC




CARRIER TAPE DIMENSION FOR 8SOICN

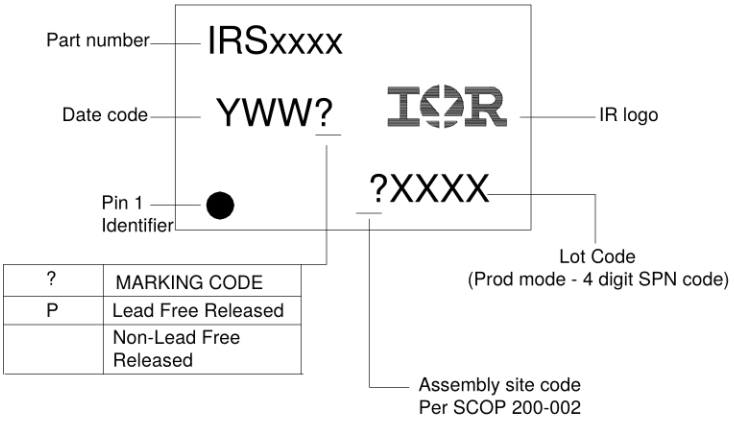
| | Metric | | Imperial | |
|---|---|---|---|---|
| Code | Min | Max | Min | Max |
| A | 7.90 | 8.10 | 0.311 | 0.318 |
| B | 3.90 | 4.10 | 0.153 | 0.161 |
| C | 11.70 | 12.30 | 0.46 | 0.484 |
| D | 5.45 | 5.55 | 0.214 | 0.218 |
| E | 6.30 | 6.50 | 0.248 | 0.255 |
| F | 5.10 | 5.30 | 0.200 | 0.208 |
| G | 1.50 | n/a | 0.059 | n/a |
| H | 1.50 | 1.60 | 0.059 | 0.062 |




REEL DIMENSIONS FOR 8SOICN

| | Metric | | Imperial | |
|---|---|---|---|---|
| Code | Min | Max | Min | Max |
| A | 329.60 | 330.25 | 12.976 | 13.001 |
| B | 20.95 | 21.45 | 0.824 | 0.844 |
| C | 12.80 | 13.20 | 0.503 | 0.519 |
| D | 1.95 | 2.45 | 0.767 | 0.096 |
| E | 98.00 | 102.00 | 3.858 | 4.015 |
| F | n/a | 18.40 | n/a | 0.724 |
| G | 14.50 | 17.10 | 0.570 | 0.673 |
| H | 12.40 | 14.40 | 0.488 | 0.566 |

## LEADFREE PART MARKING INFORMATION




| ? | MARKING CODE |
|---|---|
| P | Lead Free Released |
| | Non-Lead Free Released |

## ORDER INFORMATION

8-Lead PDIP IRS2111PbF
8-Lead SOIC IRS2111SPbF
8-Lead SOIC Tape & Reel IRS2111STRPbF

International
IOR Rectifier

**The SOIC-8 is MSL2 qualified.**
**The SOIC-14 is MSL3 qualified.**
**This product has been designed and qualified for the industrial level.**
**Qualification standards can be found at www.irf.com**

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105
Data and specifications subject to change without notice. 12/4/2006