



PSMN038-100YL

N-channel 100 V 37.5 mΩ logic level MOSFET in LFPAK56

1 May 2013

Product data sheet

1. General description

Logic level gate drive N-channel enhancement mode Field-Effect Transistor (FET) in LFPAK56 package. This product has been designed and qualified for use in a wide range of industrial, communications and domestic equipment.

2. Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for logic level gate drive
- LFPAK56 package is footprint compatible with other Power-SO8 types
- Qualified to 175 °C

3. Applications

- DC-to-DC converters
- Load switch
- TV power supplies

4. Quick reference data

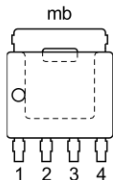
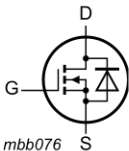
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	100	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}; \text{Fig. 1}$	-	-	30	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}; \text{Fig. 2}$	-	-	94.9	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 5\text{ A}; T_j = 175\text{ °C}; \text{Fig. 13}; \text{Fig. 12}$	-	-	103.5	mΩ
		$V_{GS} = 10\text{ V}; I_D = 5\text{ A}; T_j = 25\text{ °C}; \text{Fig. 12}$	-	30.2	37.5	mΩ
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$V_{GS} = 5\text{ V}; I_D = 5\text{ A}; V_{DS} = 80\text{ V}; T_j = 25\text{ °C}; \text{Fig. 14}; \text{Fig. 15}$	-	21.6	-	nC
Q_{GD}	gate-drain charge	$V_{GS} = 10\text{ V}; I_D = 5\text{ A}; V_{DS} = 80\text{ V}; T_j = 25\text{ °C}; \text{Fig. 14}; \text{Fig. 15}$	-	8.3	-	nC

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 30\text{ A}$; $V_{sup} \leq 100\text{ V}$; $R_{GS} = 50\ \Omega$; $V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$; unclamped; Fig. 3	-	-	45.1	mJ

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LFAK56; Power-SO8 (SOT669)</p>	 <p><i>mbb076</i></p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN038-100YL	LFAK56; Power-SO8	Plastic single-ended surface-mounted package (LFAK56; Power-SO8); 4 leads	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN038-100YL	038100

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ }^\circ\text{C}$; $T_j \leq 175\text{ }^\circ\text{C}$	-	100	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	100	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$T_{mb} = 25\text{ }^\circ\text{C}$; $V_{GS} = 10\text{ V}$; Fig. 1	-	30	A

Symbol	Parameter	Conditions	Min	Max	Unit
		$T_{mb} = 100\text{ °C}$; $V_{GS} = 10\text{ V}$; Fig. 1	-	21.3	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Fig. 4	-	120	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 2	-	94.9	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	-	79	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$	-	120	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 30\text{ A}$; $V_{sup} \leq 100\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped; Fig. 3	-	45.1	mJ

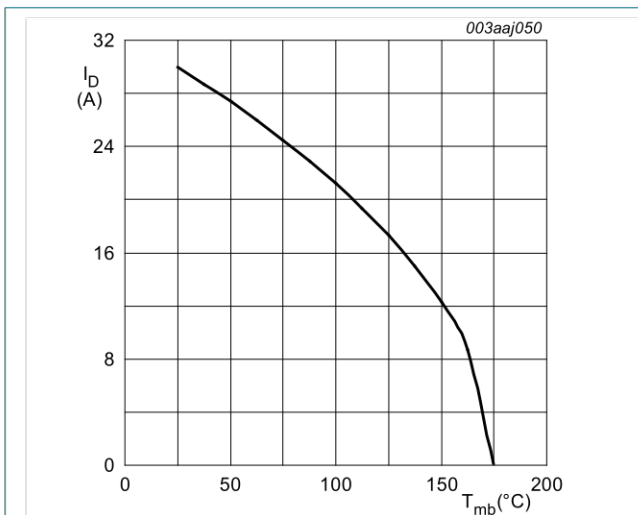


Fig. 1. Continuous drain current as a function of mounting base temperature

$$\overline{V_{GS}} \geq 10V$$

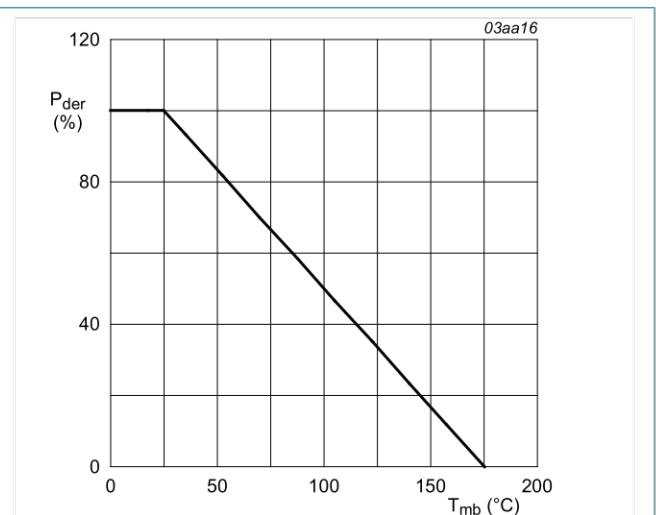


Fig. 2. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25\text{ °C})}} \times 100\%$$

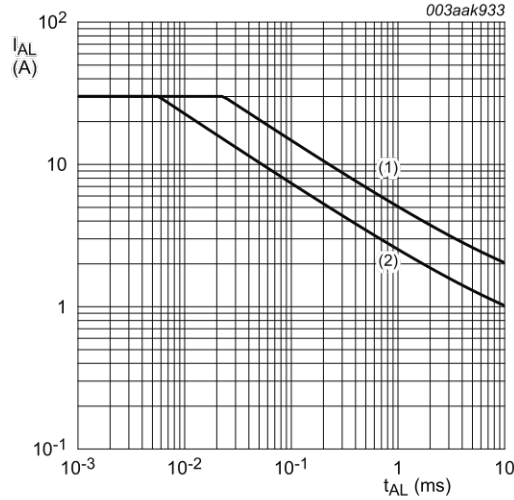


Fig. 3. Avalanche rating; avalanche current as a function of avalanche time

(1) $T_{j (avg)} = 25^{\circ}C$; (2) $T_{j (avg)} = 100^{\circ}C$

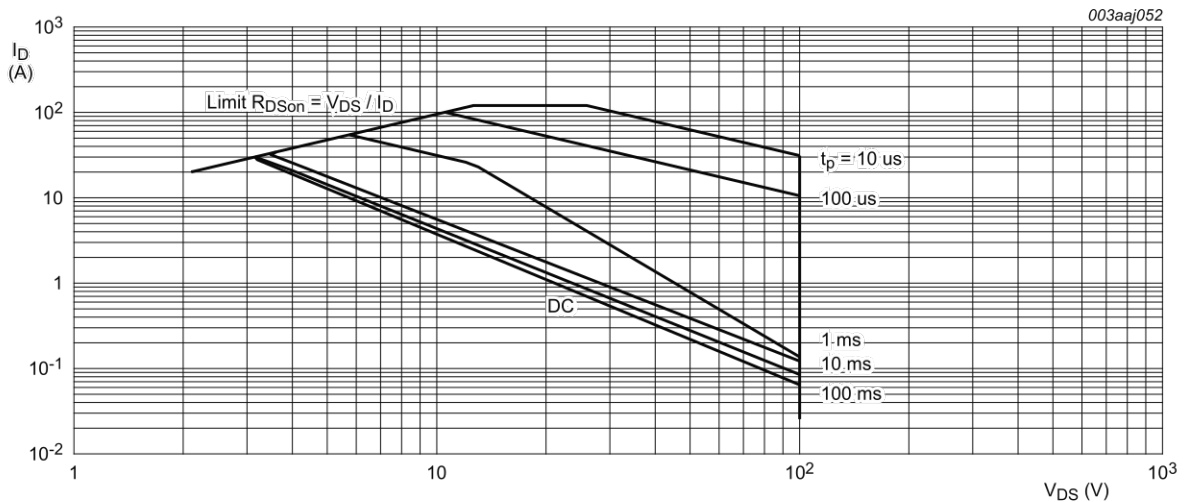


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^{\circ}C$; I_{DM} is a single pulse

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	1.44	1.58	K/W

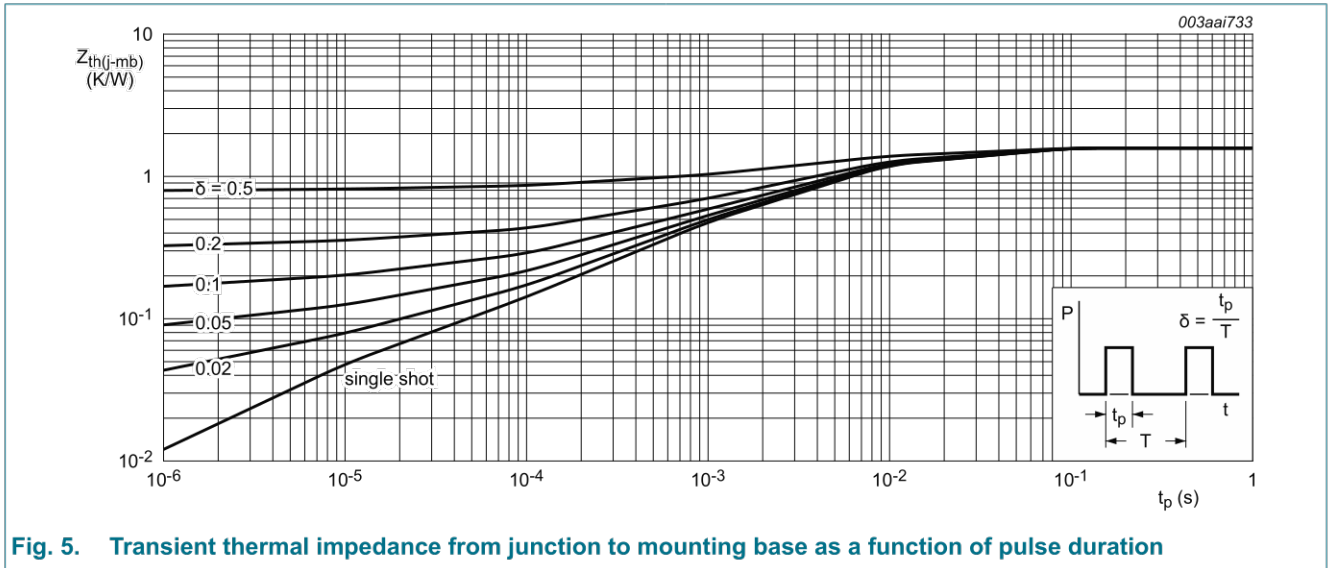


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

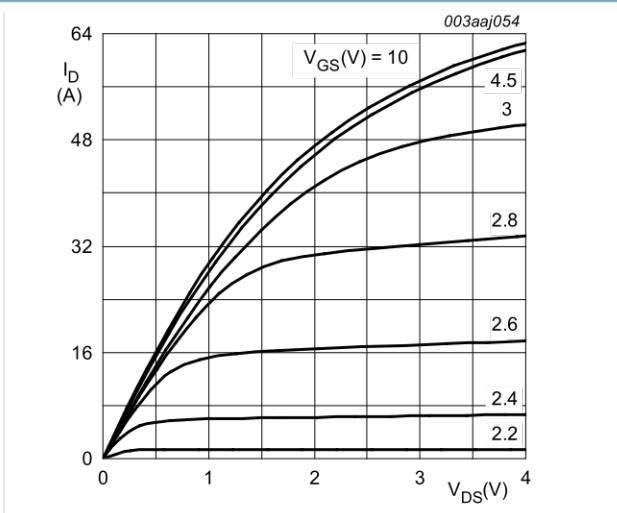
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	100	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C;$ Fig. 10 ; Fig. 11	1.4	1.7	2.1	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C;$ Fig. 10	-	-	2.45	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C;$ Fig. 10	0.5	-	-	V
I_{DSS}	drain leakage current	$V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	0.02	1	μA
		$V_{DS} = 100 V; V_{GS} = 0 V; T_j = 175 \text{ }^\circ C$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	100	nA
		$V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 5 V; I_D = 5 A; T_j = 25 \text{ }^\circ C;$ Fig. 12	-	31.3	38	mΩ
		$V_{GS} = 10 V; I_D = 5 A; T_j = 175 \text{ }^\circ C;$ Fig. 13 ; Fig. 12	-	-	103.5	mΩ
		$V_{GS} = 10 V; I_D = 5 A; T_j = 25 \text{ }^\circ C;$ Fig. 12	-	30.2	37.5	mΩ
		$V_{GS} = 5 V; I_D = 5 A; T_j = 175 \text{ }^\circ C;$ Fig. 13 ; Fig. 12	-	-	105	mΩ
R_G	gate resistance	$f = 1 \text{ MHz}$	-	1.64	-	Ω

N-channel 100 V 37.5 mΩ logic level MOSFET in LFPAK56

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 5 A; V _{DS} = 80 V; V _{GS} = 10 V; T _j = 25 °C; Fig. 14 ; Fig. 15	-	39.2	-	nC
		I _D = 5 A; V _{DS} = 80 V; V _{GS} = 5 V; T _j = 25 °C; Fig. 14 ; Fig. 15	-	21.6	-	nC
Q _{GS}	gate-source charge	I _D = 5 A; V _{DS} = 80 V; V _{GS} = 10 V; T _j = 25 °C; Fig. 14 ; Fig. 15	-	3.8	-	nC
Q _{GD}	gate-drain charge		-	8.3	-	nC
Q _{GS(th)}	pre-threshold gate-source charge		-	2.7	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge		-	1.1	-	nC
V _{GS(pl)}	gate-source plateau voltage	I _D = 5 A; V _{DS} = 80 V; T _j = 25 °C; Fig. 14 ; Fig. 15	-	2.3	-	V
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz; T _j = 25 °C; Fig. 16	-	1905	-	pF
C _{oss}	output capacitance		-	137	-	pF
C _{rss}	reverse transfer capacitance		-	90	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 80 V; R _L = 10 Ω; V _{GS} = 5 V; R _{G(ext)} = 5 Ω; T _j = 25 °C	-	10	-	ns
t _r	rise time		-	18	-	ns
t _{d(off)}	turn-off delay time		-	31	-	ns
t _f	fall time		-	18	-	ns
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 5 A; V _{GS} = 0 V; T _j = 25 °C; Fig. 17	-	0.78	1.2	V
t _{rr}	reverse recovery time	I _S = 10 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 25 V; T _j = 25 °C	-	31	-	ns
Q _r	recovered charge		-	44	-	nC



$T_j = 25^\circ C; t_p = 300 \mu s$

Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

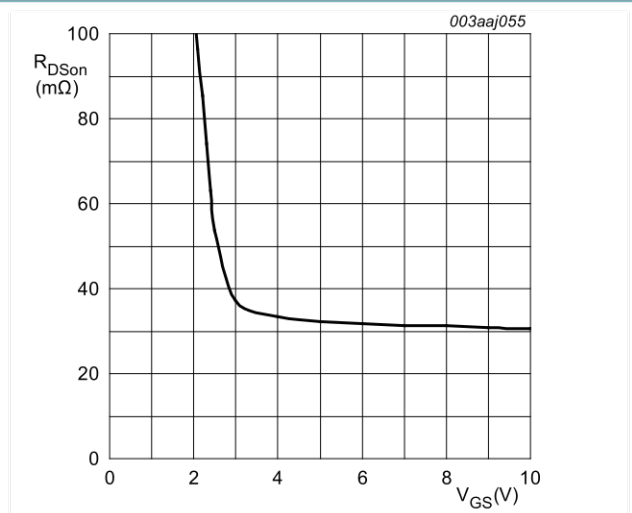


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25^\circ C; I_D = 5A$

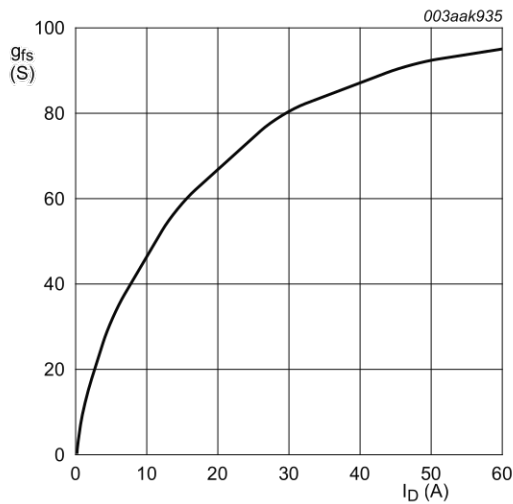


Fig. 8. Forward transconductance as a function of drain current; typical values

$T_j = 25^\circ C; V_{DS} = 10V$

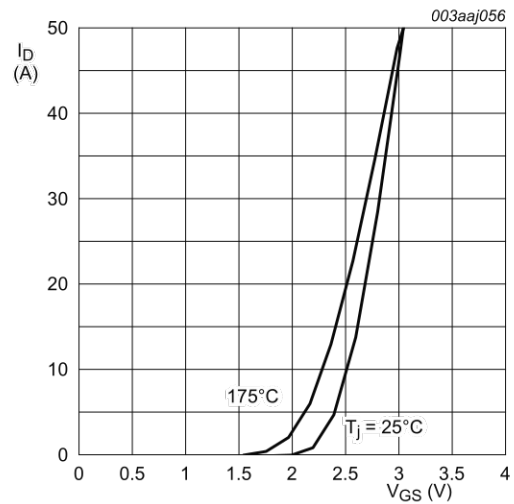


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10V$

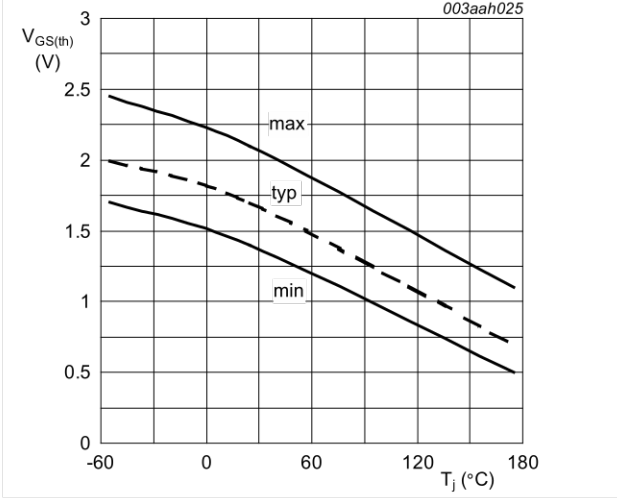


Fig. 10. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$$

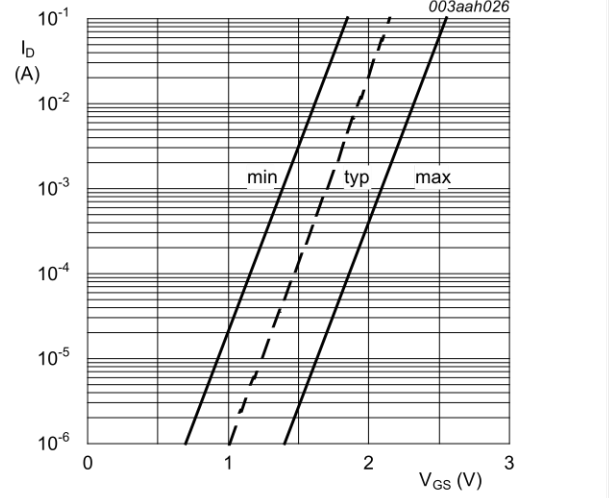
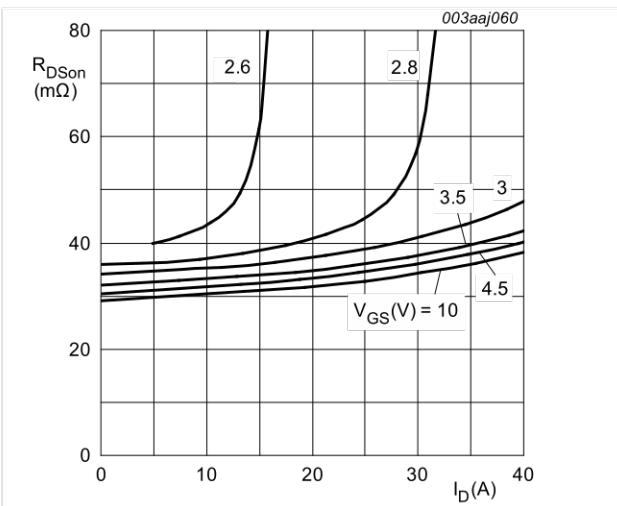


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$$



$$T_j = 25^\circ\text{C}; t_p = 300 \mu\text{s}$$

Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

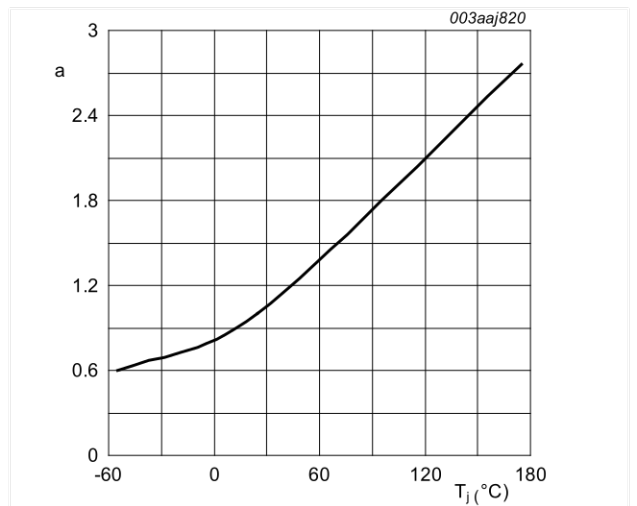


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$$\alpha = \frac{R_{DS(on)}}{R_{DS(on)}(25^\circ\text{C})}$$

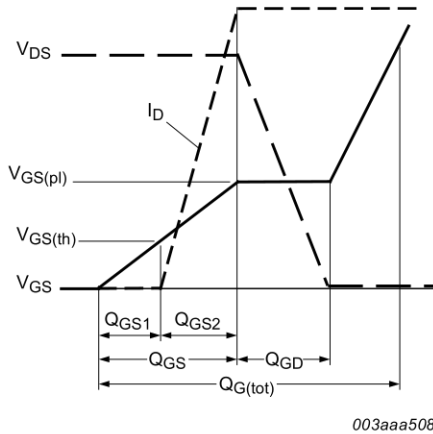


Fig. 14. Gate charge waveform definitions

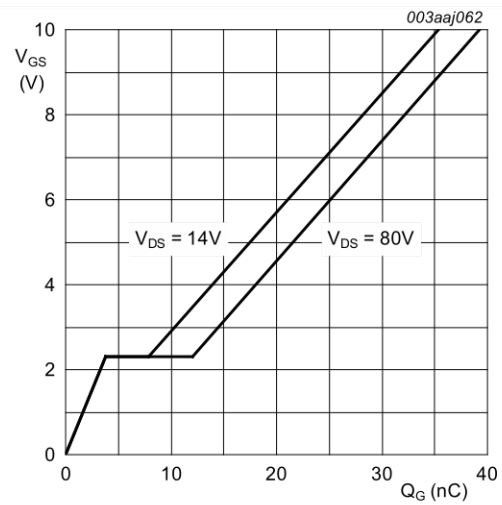


Fig. 15. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25^\circ C; I_D = 5A$$

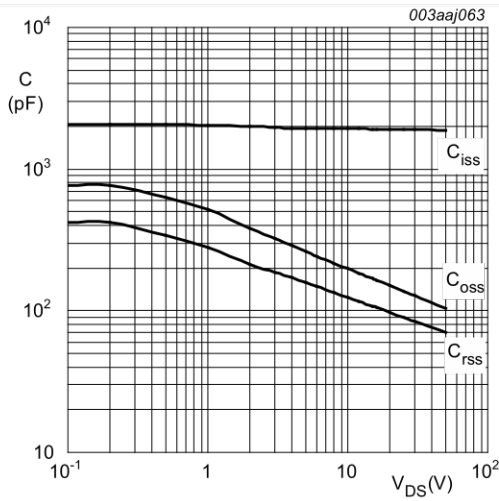


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0V; f = 1MHz$$

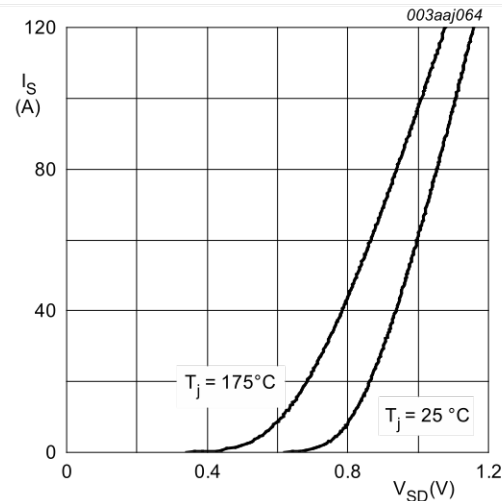


Fig. 17. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$$V_{GS} = 0V$$

11. Package outline

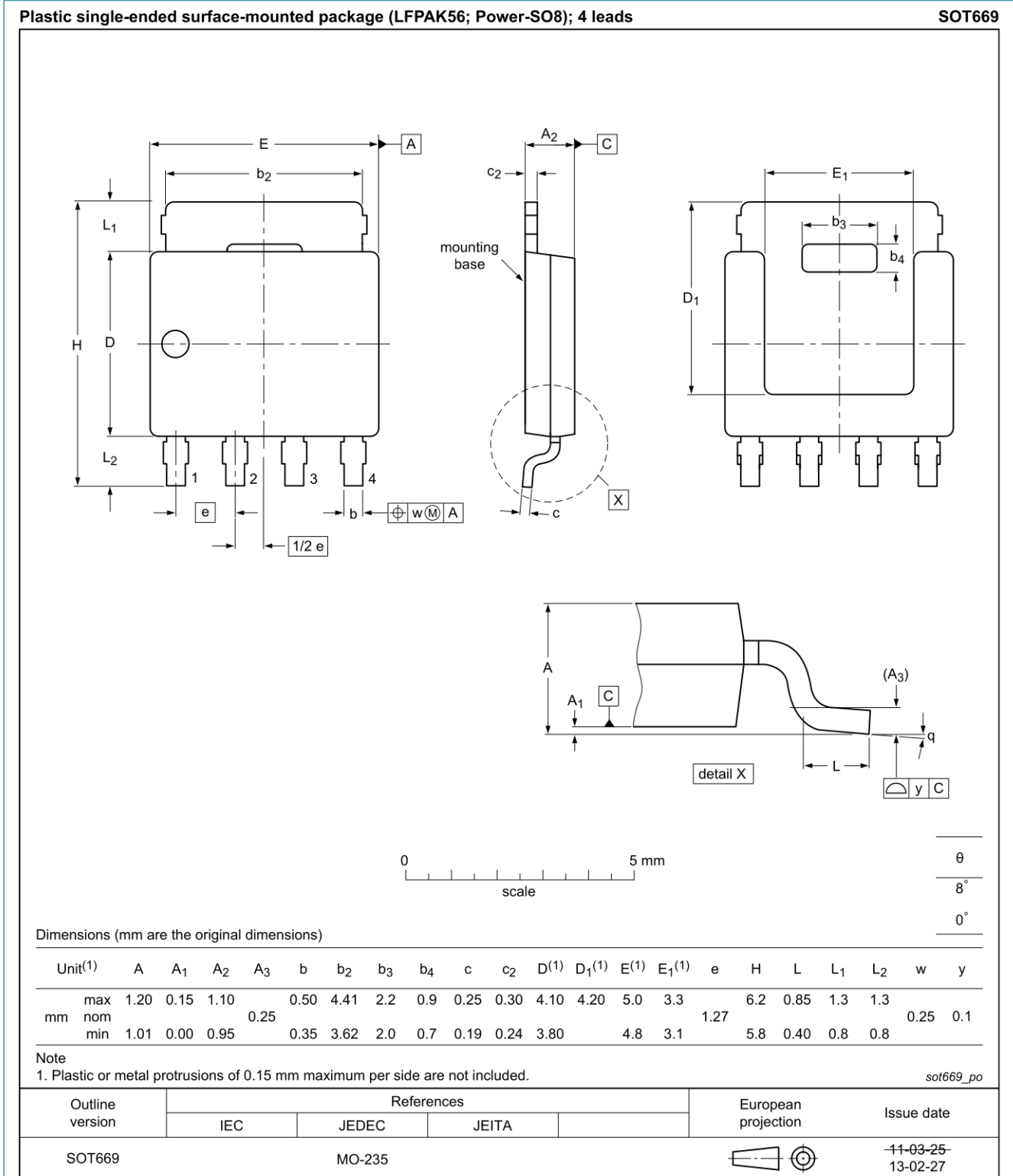


Fig. 18. Package outline LPAK56; Power-SO8 (SOT669)

12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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