

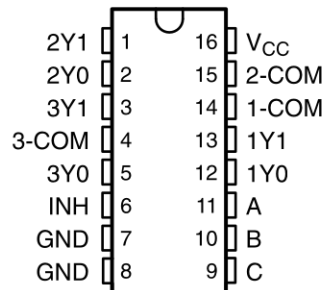
SN54LV4053A, SN74LV4053A

TRIPLE 2-CHANNEL ANALOG MULTIPLEXERS/DEMULTEPLEXERS

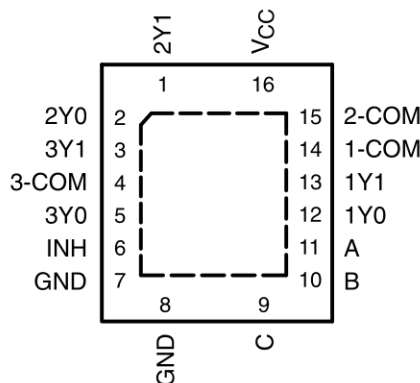
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- 2-V to 5.5-V V_{CC} Operation
- Support Mixed-Mode Voltage Operation on All Ports
- High On-Off Output-Voltage Ratio
- Low Crosstalk Between Switches
- Individual Switch Controls
- Extremely Low Input Current
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

SN54LV4053A . . . J OR W PACKAGE
SN74LV4053A . . . D, DB, DGV, N, NS, OR PW PACKAGE
(TOP VIEW)



SN74LV4053A . . . RGY PACKAGE
(TOP VIEW)



description/ordering information

These triple 2-channel CMOS analog multiplexers/demultiplexers are designed for 2-V to 5.5-V V_{CC} operation.

The 'LV4053A devices handle both analog and digital signals. Each channel permits signals with amplitudes up to 5.5 V (peak) to be transmitted in either direction.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING | |
|----------------|--------------|-----------------|-----------------------|------------------|----------------|
| –40°C to 85°C | PDIP – N | Tube of 25 | SN74LV4053AN | SN74LV4053AN | |
| | QFN – RGY | Reel of 1000 | SN74LV4053ARGYR | LW053A | |
| | SOIC – D | Tube of 40 | SN74LV4053AD | LV4053A | |
| | | Reel of 2500 | SN74LV4053ADR | | |
| | SOP – NS | Reel of 2000 | SN74LV4053ANSR | 74LV4053A | |
| | SSOP – DB | Tube of 90 | SN74LV4053APW | LW053A | |
| | | | Reel of 2000 | | SN74LV4053APWR |
| | | | Reel of 250 | | SN74LV4053APWT |
| TVSOP – DGV | Reel of 2000 | SN74LV4053ADGVR | LW053A | | |
| –55°C to 125°C | CDIP – J | Tube of 25 | SNJ54LV4053AJ | SNJ54LV4053AJ | |
| | CFP – W | Tube of 150 | SNJ54LV4053AW | SNJ54LV4053AW | |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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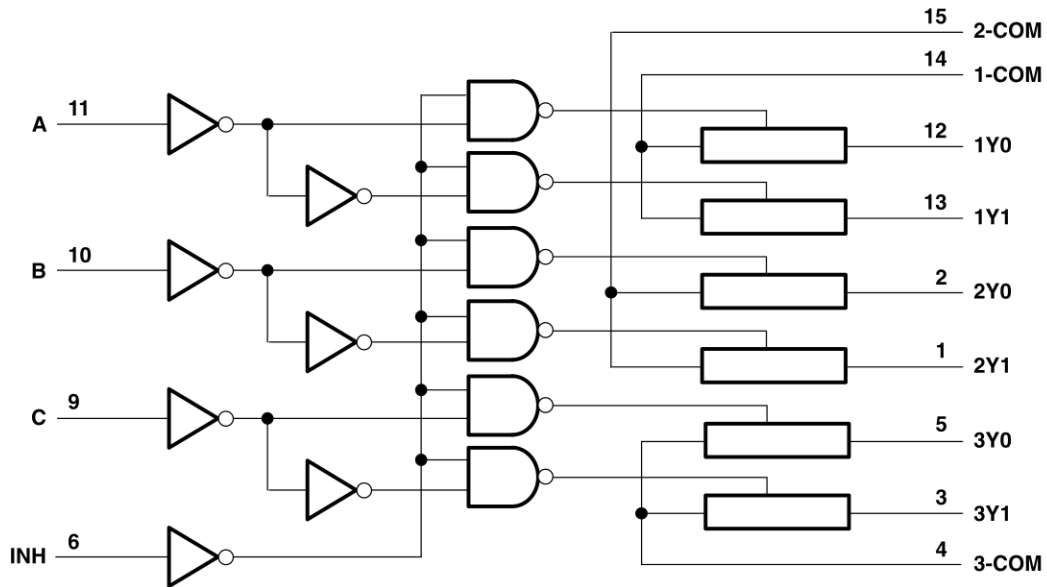
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FUNCTION TABLE

| INPUTS | | | | ON CHANNELS |
|--------|---|---|---|---------------|
| INH | C | B | A | |
| L | L | L | L | 1Y0, 2Y0, 3Y0 |
| L | L | L | H | 1Y1, 2Y0, 3Y0 |
| L | L | H | L | 1Y0, 2Y1, 3Y0 |
| L | L | H | H | 1Y1, 2Y1, 3Y0 |
| L | H | L | L | 1Y0, 2Y0, 3Y1 |
| L | H | L | H | 1Y1, 2Y0, 3Y1 |
| L | H | H | L | 1Y0, 2Y1, 3Y1 |
| L | H | H | H | 1Y1, 2Y1, 3Y1 |
| H | X | X | X | None |

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|----------------------------|
| Supply voltage range, V_{CC} | –0.5 V to 7 V |
| Input voltage range, V_I (see Note 1) | –0.5 V to 7 V |
| Switch I/O voltage range, V_{IO} (see Notes 1 and 2) | –0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, I_{IK} ($V_I < 0$) | –20 mA |
| I/O diode current, I_{IOK} ($V_{IO} < 0$) | –50 mA |
| Switch through current, I_T ($V_{IO} = 0$ to V_{CC}) | ±25 mA |
| Continuous current through V_{CC} or GND | ±50 mA |
| Package thermal impedance, θ_{JA} (see Note 3): D package | 73°C/W |
| (see Note 3): DB package | 82°C/W |
| (see Note 3): DGV package | 120°C/W |
| (see Note 3): NS package | 64°C/W |
| (see Note 3): PW package | 108°C/W |
| (see Note 4): RGY package | 39°C/W |
| Storage temperature range, T_{stg} | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 5.5 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.
 4. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 5)

| | | SN54LV4053A | | SN74LV4053A | | UNIT |
|---------------------|--|---------------------------|---------------------|---------------------|----------|------|
| | | MIN | MAX | MIN | MAX | |
| V_{CC} | Supply voltage | 2‡ | 5.5 | 2‡ | 5.5 | V |
| V_{IH} | High-level input voltage, control inputs | $V_{CC} = 2$ V | 1.5 | 1.5 | | V |
| | | $V_{CC} = 2.3$ V to 2.7 V | $V_{CC} \times 0.7$ | $V_{CC} \times 0.7$ | | |
| | | $V_{CC} = 3$ V to 3.6 V | $V_{CC} \times 0.7$ | $V_{CC} \times 0.7$ | | |
| | | $V_{CC} = 4.5$ V to 5.5 V | $V_{CC} \times 0.7$ | $V_{CC} \times 0.7$ | | |
| V_{IL} | Low-level input voltage, control inputs | $V_{CC} = 2$ V | 0.5 | 0.5 | | V |
| | | $V_{CC} = 2.3$ V to 2.7 V | $V_{CC} \times 0.3$ | $V_{CC} \times 0.3$ | | |
| | | $V_{CC} = 3$ V to 3.6 V | $V_{CC} \times 0.3$ | $V_{CC} \times 0.3$ | | |
| | | $V_{CC} = 4.5$ V to 5.5 V | $V_{CC} \times 0.3$ | $V_{CC} \times 0.3$ | | |
| V_I | Control input voltage | 0 | 5.5 | 0 | 5.5 | V |
| V_{IO} | Input/output voltage | 0 | V_{CC} | 0 | V_{CC} | V |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC} = 2.3$ V to 2.7 V | 200 | 200 | | ns/V |
| | | $V_{CC} = 3$ V to 3.6 V | 100 | 100 | | |
| | | $V_{CC} = 4.5$ V to 5.5 V | 20 | 20 | | |
| T_A | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

‡ With supply voltages at or near 2 V, the analog switch on-state resistance becomes very nonlinear. It is recommended that only digital signals be transmitted at these low supply voltages.

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | SN54LV4053A | | SN74LV4053A | | UNIT | |
|---|---|-----------------|-----------------------|-----|-----|-------------|------|-------------|-----|------|----|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | | |
| r _{on} On-state switch resistance | I _T = 2 mA, V _I = V _{CC} or GND, V _{INH} = V _{IL} (see Figure 1) | 2.3 V | | 41 | 180 | | 225 | | 225 | Ω | |
| | | 3 V | | 30 | 150 | | 190 | | 190 | | |
| | | 4.5 V | | 23 | 75 | | 100 | | 100 | | |
| r _{on(p)} Peak on-state resistance | I _T = 2 mA, V _I = V _{CC} to GND, V _{INH} = V _{IL} | 2.3 V | | 139 | 500 | | 600 | | 600 | Ω | |
| | | 3 V | | 63 | 180 | | 225 | | 225 | | |
| | | 4.5 V | | 35 | 100 | | 125 | | 125 | | |
| Δr _{on} Difference in on-state resistance between switches | I _T = 2 mA, V _I = V _{CC} to GND, V _{INH} = V _{IL} | 2.3 V | | 2 | 30 | | 40 | | 40 | Ω | |
| | | 3 V | | 1.6 | 20 | | 30 | | 30 | | |
| | | 4.5 V | | 1.3 | 15 | | 20 | | 20 | | |
| I _I Control input current | V _I = 5.5 V or GND | 0 to 5.5 V | | | | | ±0.1 | | ±1 | ±1 | μA |
| I _{S(off)} Off-state switch leakage current | V _I = V _{CC} and V _O = GND, or V _I = GND and V _O = V _{CC} , V _{INH} = V _{IH} (see Figure 2) | 5.5 V | | | | | ±0.1 | | ±1 | ±1 | μA |
| I _{S(on)} On-state switch leakage current | V _I = V _{CC} or GND, V _{INH} = V _{IH} (see Figure 3) | 5.5 V | | | | | ±0.1 | | ±1 | ±1 | μA |
| I _{CC} Supply current | V _I = V _{CC} or GND | 5.5 V | | | | | | 20 | | 20 | μA |
| C _{IC} Control input capacitance | | | | | 2 | | | | | | pF |
| C _{IS} Common terminal capacitance | | | | | 8.2 | | | | | | pF |
| C _{OS} Switch terminal capacitance | | | | | 5.6 | | | | | | pF |
| C _F Feedthrough capacitance | | | | | 0.5 | | | | | | pF |

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | T _A = 25°C | | | SN54LV4053A | | SN74LV4053A | | UNIT |
|---|-----------------------|-----------------------|---------------------------------------|-----------------------|------|-----|-------------|-----|-------------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t _{PLH} Propagation delay time | COM or Y _n | Y _n or COM | C _L = 15 pF (see Figure 4) | | 2.5 | 10 | | 16 | | 16 | ns |
| t _{PZH} Enable delay time | INH | COM or Y _n | C _L = 15 pF (see Figure 5) | | 7.6 | 18 | | 23 | | 23 | ns |
| t _{PZL} Disable delay time | INH | COM or Y _n | C _L = 15 pF (see Figure 5) | | 7.7 | 18 | | 23 | | 23 | ns |
| t _{PLH} Propagation delay time | COM or Y _n | Y _n or COM | C _L = 50 pF (see Figure 4) | | 4.4 | 12 | | 18 | | 18 | ns |
| t _{PZH} Enable delay time | INH | COM or Y _n | C _L = 50 pF (see Figure 5) | | 8.8 | 28 | | 35 | | 35 | ns |
| t _{PZL} Disable delay time | INH | COM or Y _n | C _L = 50 pF (see Figure 5) | | 11.7 | 28 | | 35 | | 35 | ns |

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | T _A = 25°C | | | SN54LV4053A | | SN74LV4053A | | UNIT |
|--------------------------------------|------------------------|-------------|-----------------|--|-----|-----|-------------|-----|-------------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t _{PLH} t _{PHL} | Propagation delay time | COM or Yn | Yn or COM | C _L = 15 pF (see Figure 4) | 1.6 | 6 | 10 | 10 | 10 | 10 | ns |
| t _{PZH} t _{PZL} | Enable delay time | INH | COM or Yn | C _L = 15 pF (see Figure 5) | 5.3 | 12 | 15 | 15 | 15 | 15 | ns |
| t _{PHZ} t _{PLZ} | Disable delay time | INH | COM or Yn | C _L = 15 pF (see Figure 5) | 6.1 | 12 | 15 | 15 | 15 | 15 | ns |
| t _{PLH} t _{PHL} | Propagation delay time | COM or Yn | Yn or COM | C _L = 50 pF (see Figure 4) | 2.9 | 9 | 12 | 12 | 12 | 12 | ns |
| t _{PZH} t _{PZL} | Enable delay time | INH | COM or Yn | C _L = 50 pF (see Figure 5) | 6.1 | 20 | 25 | 25 | 25 | 25 | ns |
| t _{PHZ} t _{PLZ} | Disable delay time | INH | COM or Yn | C _L = 50 pF (see Figure 5) | 8.9 | 20 | 25 | 25 | 25 | 25 | ns |

**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | T _A = 25°C | | | SN54LV4053A | | SN74LV4053A | | UNIT |
|--------------------------------------|------------------------|-------------|-----------------|--|-----|-----|-------------|-----|-------------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t _{PLH} t _{PHL} | Propagation delay time | COM or Yn | Yn or COM | C _L = 15 pF (see Figure 4) | 0.9 | 4 | 7 | 7 | 7 | 7 | ns |
| t _{PZH} t _{PZL} | Enable delay time | INH | COM or Yn | C _L = 15 pF (see Figure 5) | 3.8 | 8 | 10 | 10 | 10 | 10 | ns |
| t _{PHZ} t _{PLZ} | Disable delay time | INH | COM or Yn | C _L = 15 pF (see Figure 5) | 4.6 | 8 | 10 | 10 | 10 | 10 | ns |
| t _{PLH} t _{PHL} | Propagation delay time | COM or Yn | Yn or COM | C _L = 50 pF (see Figure 4) | 1.8 | 6 | 8 | 8 | 8 | 8 | ns |
| t _{PZH} t _{PZL} | Enable delay time | INH | COM or Yn | C _L = 50 pF (see Figure 5) | 4.3 | 14 | 18 | 18 | 18 | 18 | ns |
| t _{PHZ} t _{PLZ} | Disable delay time | INH | COM or Yn | C _L = 50 pF (see Figure 5) | 6.3 | 14 | 18 | 18 | 18 | 18 | ns |

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analog switch characteristics

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | V _{CC} | T _A = 25°C | UNIT | |
|--|-----------------------|-----------------------|--|---------------------------------------|-----------------------|------|---|
| | | | | | TYP | | |
| Frequency response (switch on) | COM or Y _n | Y _n or COM | C _L = 50 pF, R _L = 600 Ω, f _{in} = 1 MHz (sine wave) (see Note 6 and Figure 6) | 2.3 V | 30 | MHz | |
| | | | | 3 V | 35 | | |
| | | | | 4.5 V | 50 | | |
| Crosstalk (between any switches) | COM or Y _n | Y _n or COM | C _L = 50 pF, R _L = 600 Ω, f _{in} = 1 MHz (sine wave) (see Note 7 and Figure 7) | 2.3 V | -45 | dB | |
| | | | | 3 V | -45 | | |
| | | | | 4.5 V | -45 | | |
| Crosstalk (control input to signal output) | INH | COM or Y _n | C _L = 50 pF, R _L = 600 Ω, f _{in} = 1 MHz (square wave) (see Figure 8) | 2.3 V | 20 | mV | |
| | | | | 3 V | 35 | | |
| | | | | 4.5 V | 65 | | |
| Feedthrough attenuation (switch off) | COM or Y _n | Y _n or COM | C _L = 50 pF, R _L = 600 Ω, f _{in} = 1 MHz (see Note 7 and Figure 9) | 2.3 V | -45 | dB | |
| | | | | 3 V | -45 | | |
| | | | | 4.5 V | -45 | | |
| Sine-wave distortion | COM or Y _n | Y _n or COM | C _L = 50 pF, R _L = 10 kΩ, f _{in} = 1 kHz (sine wave) (see Figure 10) | V _I = 2 V _{p-p} | 2.3 V | 0.1 | % |
| | | | | V _I = 2.5 V _{p-p} | 3 V | 0.1 | |
| | | | | V _I = 4 V _{p-p} | 4.5 V | 0.1 | |

NOTES: 6. Adjust f_{in} voltage to obtain 0-dBm output. Increase f_{in} frequency until dB meter reads -3 dB.
7. Adjust f_{in} voltage to obtain 0-dBm input.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|---|------------------------------------|-----|------|
| C _{pd} Power dissipation capacitance | C _L = 50 pF, f = 10 MHz | 5.3 | pF |

PARAMETER MEASUREMENT INFORMATION

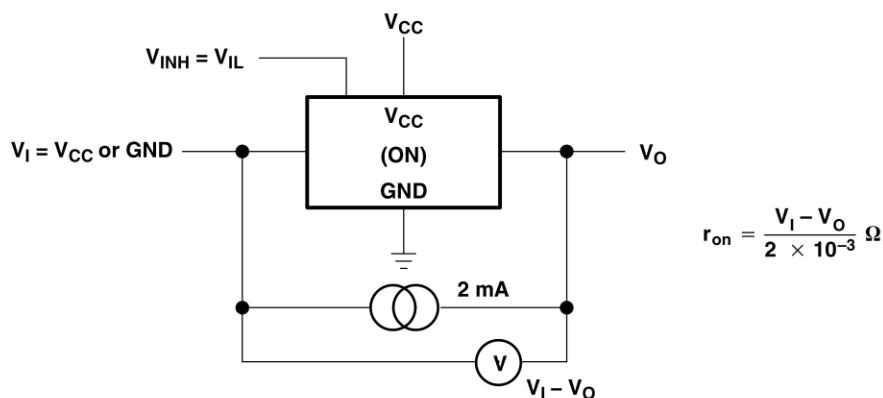


Figure 1. On-State Resistance Test Circuit

PARAMETER MEASUREMENT INFORMATION

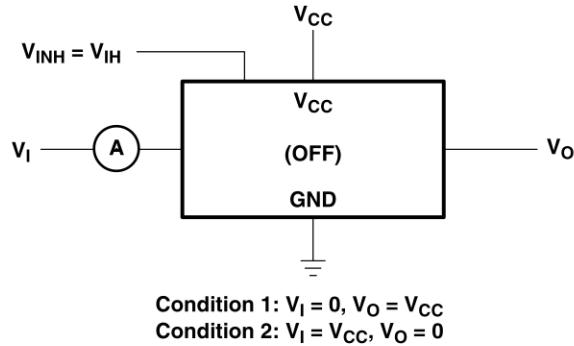


Figure 2. Off-State Switch Leakage-Current Test Circuit

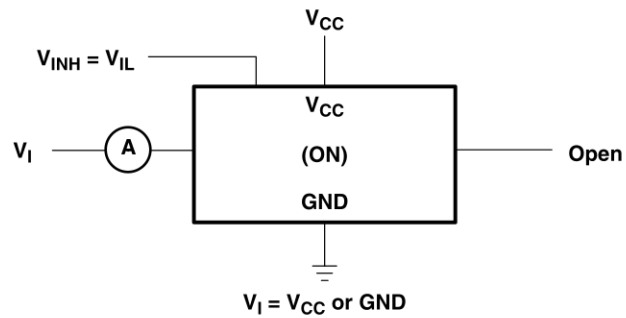


Figure 3. On-State Switch Leakage-Current Test Circuit

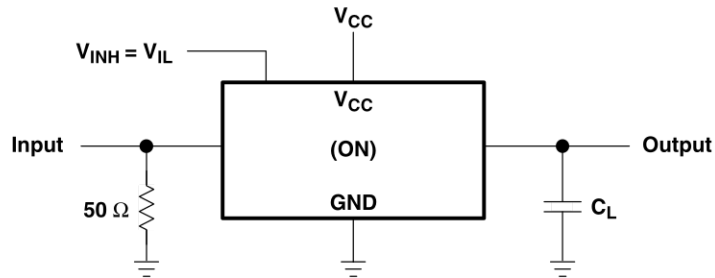


Figure 4. Propagation Delay Time, Signal Input to Signal Output

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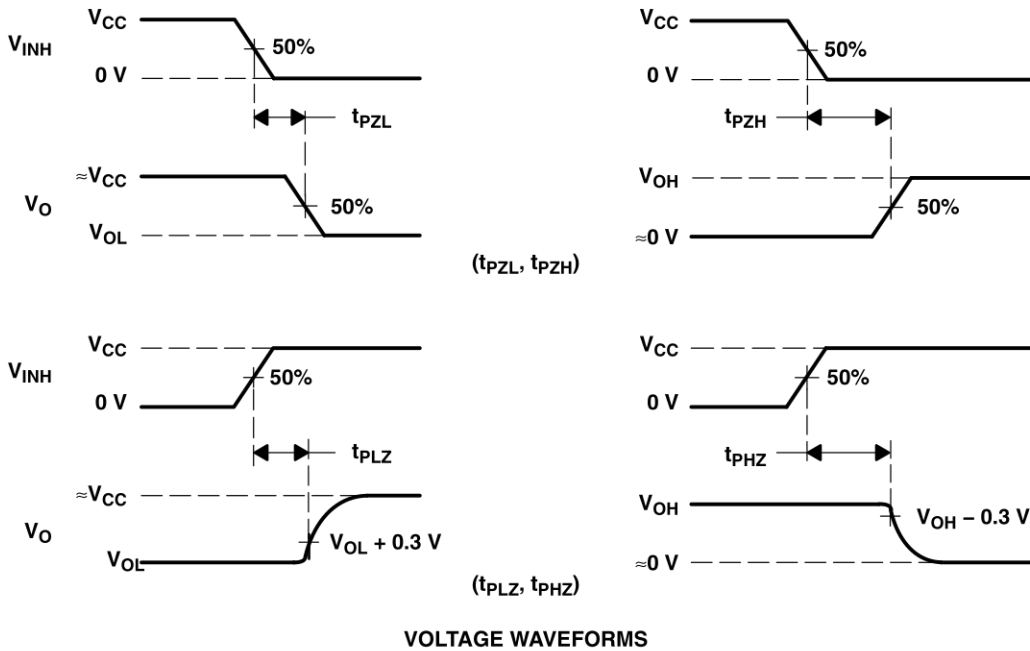
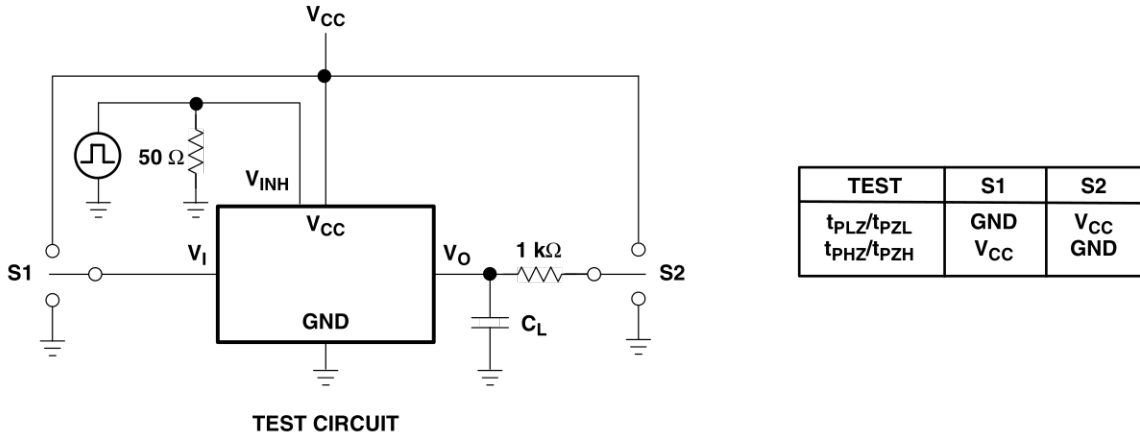
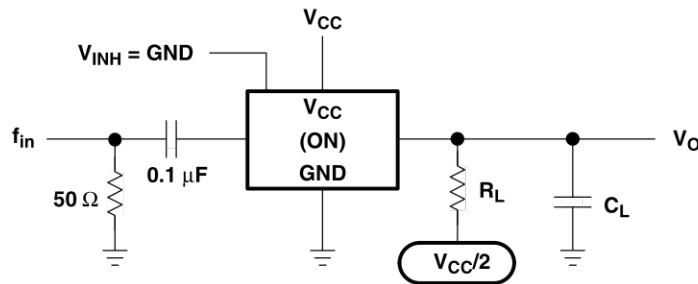


Figure 5. Switching Time (t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}), Control to Signal Output



NOTE A: f_{in} is a sine wave.

Figure 6. Frequency Response (Switch On)

PARAMETER MEASUREMENT INFORMATION

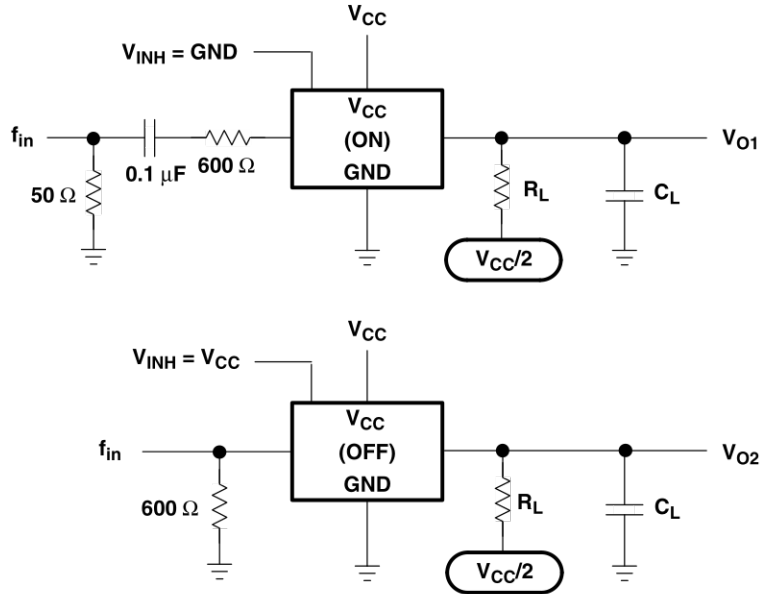


Figure 7. Crosstalk Between Any Two Switches

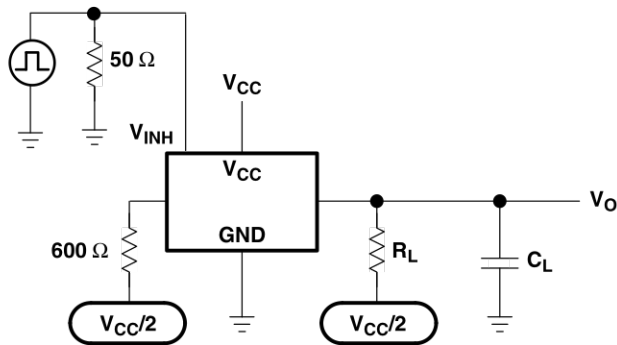


Figure 8. Crosstalk Between Control Input and Switch Output

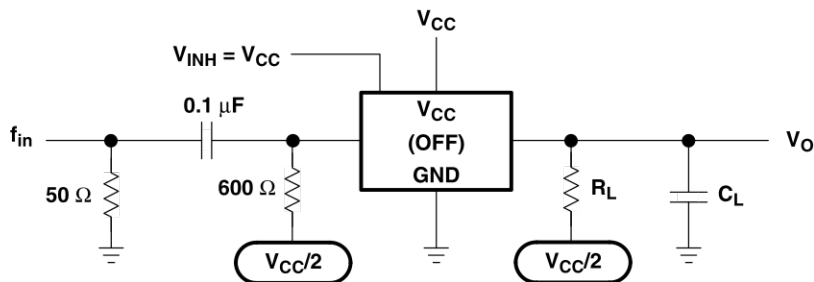


Figure 9. Feedthrough Attenuation (Switch Off)

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PARAMETER MEASUREMENT INFORMATION

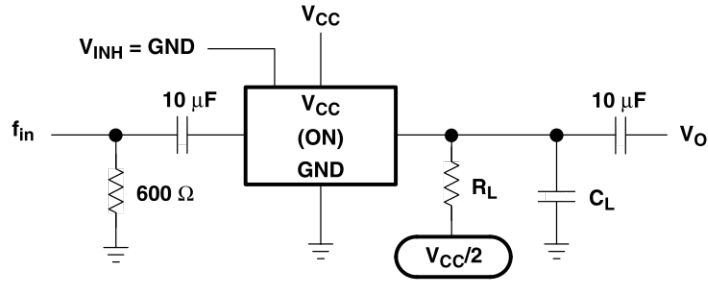


Figure 10. Sine-Wave Distortion

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| SN74LV4053AD | LIFEBUY | SOIC | D | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV4053A | |
| SN74LV4053ADBR | LIFEBUY | SSOP | DB | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LW053A | |
| SN74LV4053ADE4 | LIFEBUY | SOIC | D | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV4053A | |
| SN74LV4053ADGVR | LIFEBUY | TVSOP | DGV | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LW053A | |
| SN74LV4053ADR | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU SN | Level-1-260C-UNLIM | -40 to 85 | LV4053A | Samples |
| SN74LV4053AN | LIFEBUY | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | SN74LV4053AN | |
| SN74LV4053ANSR | LIFEBUY | SO | NS | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 74LV4053A | |
| SN74LV4053APW | LIFEBUY | TSSOP | PW | 16 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LW053A | |
| SN74LV4053APWR | ACTIVE | TSSOP | PW | 16 | 2000 | RoHS & Green | NIPDAU SN | Level-1-260C-UNLIM | -40 to 85 | LW053A | Samples |
| SN74LV4053APWRG4 | LIFEBUY | TSSOP | PW | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LW053A | |
| SN74LV4053APWT | LIFEBUY | TSSOP | PW | 16 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LW053A | |
| SN74LV4053ARGYR | ACTIVE | VQFN | RGY | 16 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | LW053A | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

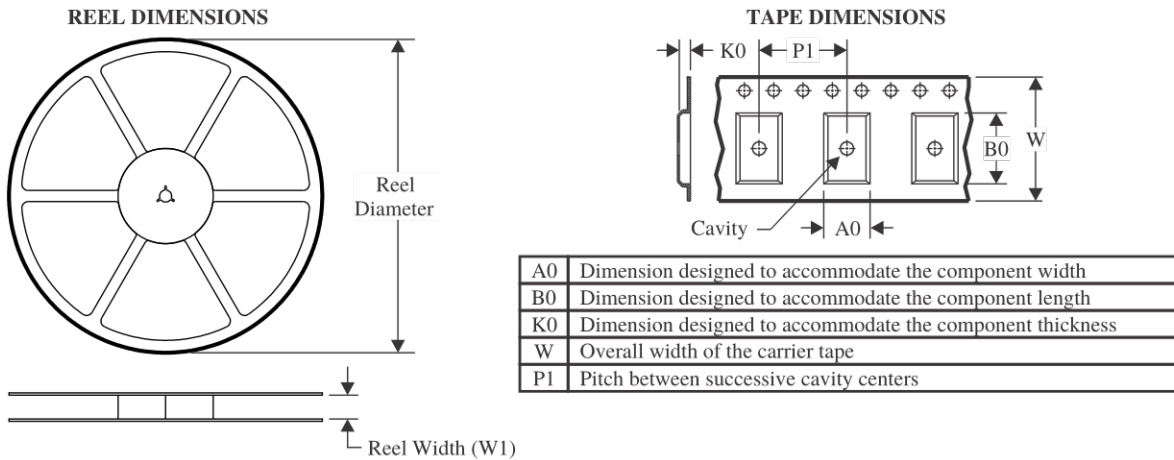
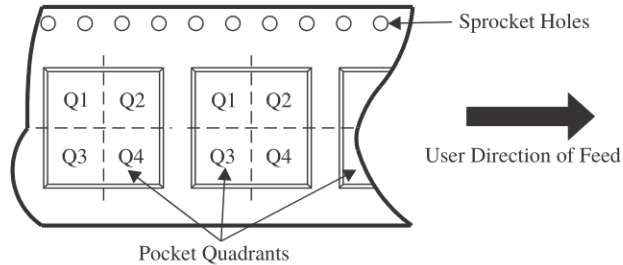
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LV4053A :

- Automotive : [SN74LV4053A-Q1](#)
- Enhanced Product : [SN74LV4053A-EP](#)

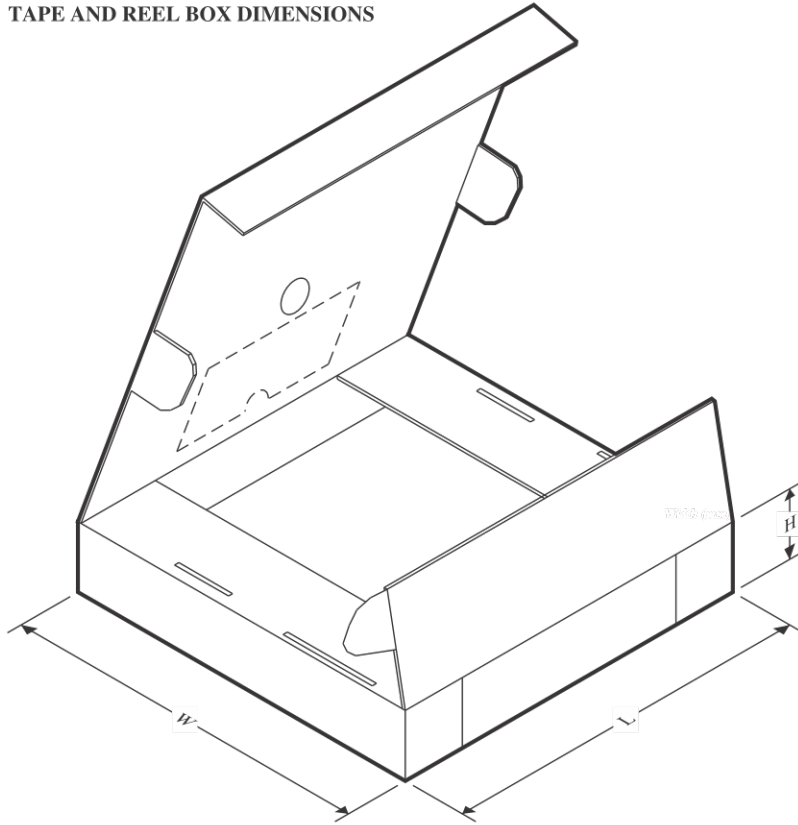
NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


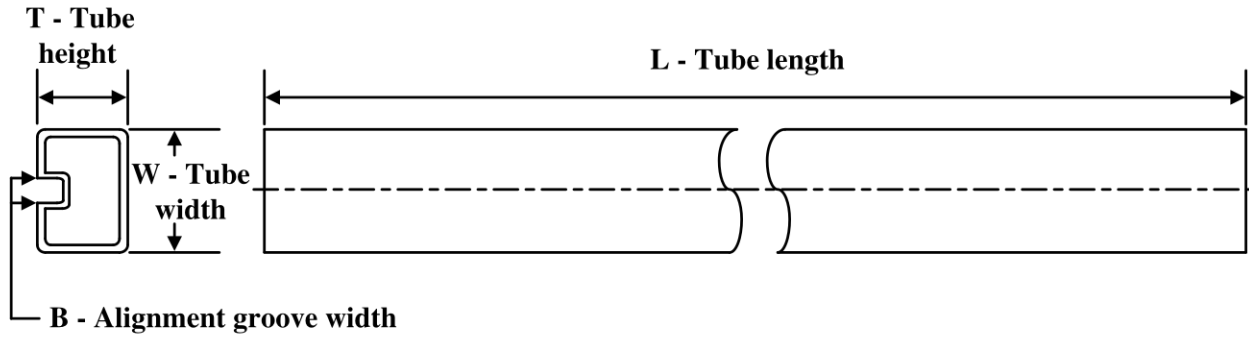
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LV4053ADBR | SSOP | DB | 16 | 2000 | 330.0 | 16.4 | 8.35 | 6.6 | 2.4 | 12.0 | 16.0 | Q1 |
| SN74LV4053ADGVR | TVSOP | DGV | 16 | 2000 | 330.0 | 12.4 | 6.8 | 4.0 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV4053ADR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LV4053ADR | SOIC | D | 16 | 2500 | 330.0 | 16.8 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LV4053ANSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LV4053APWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV4053APWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV4053APWRG4 | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV4053APWT | TSSOP | PW | 16 | 250 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV4053ARGYR | VQFN | RGY | 16 | 3000 | 330.0 | 12.4 | 3.8 | 4.3 | 1.5 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LV4053ADBR | SSOP | DB | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LV4053ADGVR | TVSOP | DGV | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LV4053ADR | SOIC | D | 16 | 2500 | 340.5 | 336.1 | 32.0 |
| SN74LV4053ADR | SOIC | D | 16 | 2500 | 364.0 | 364.0 | 27.0 |
| SN74LV4053ANSR | SO | NS | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LV4053APWR | TSSOP | PW | 16 | 2000 | 364.0 | 364.0 | 27.0 |
| SN74LV4053APWR | TSSOP | PW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LV4053APWRG4 | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74LV4053APWT | TSSOP | PW | 16 | 250 | 356.0 | 356.0 | 35.0 |
| SN74LV4053ARGYR | VQFN | RGY | 16 | 3000 | 367.0 | 367.0 | 35.0 |

TUBE


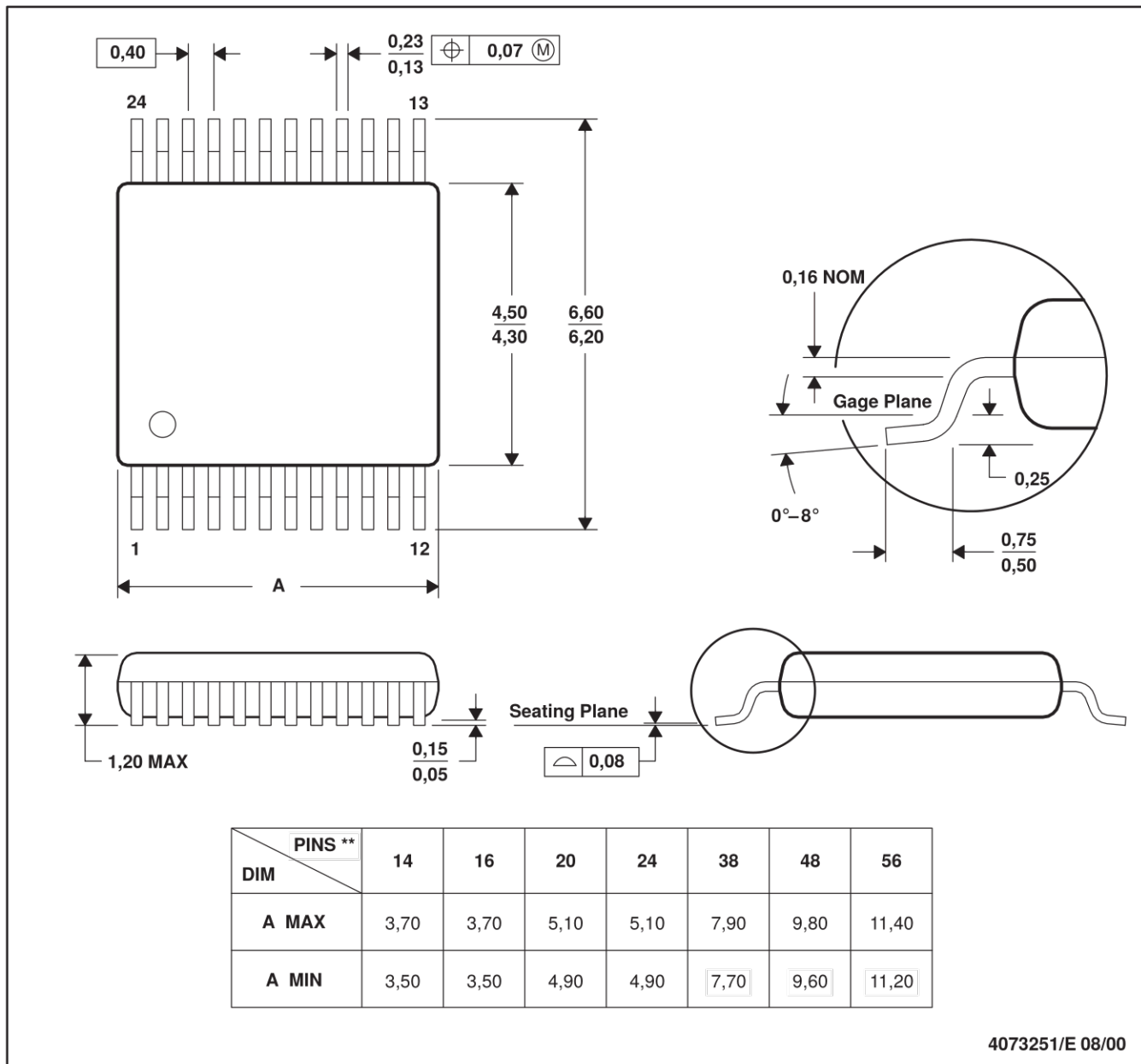
*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74LV4053AD | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |
| SN74LV4053ADE4 | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |
| SN74LV4053AN | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74LV4053AN | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74LV4053APW | PW | TSSOP | 16 | 90 | 530 | 10.2 | 3600 | 3.5 |

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

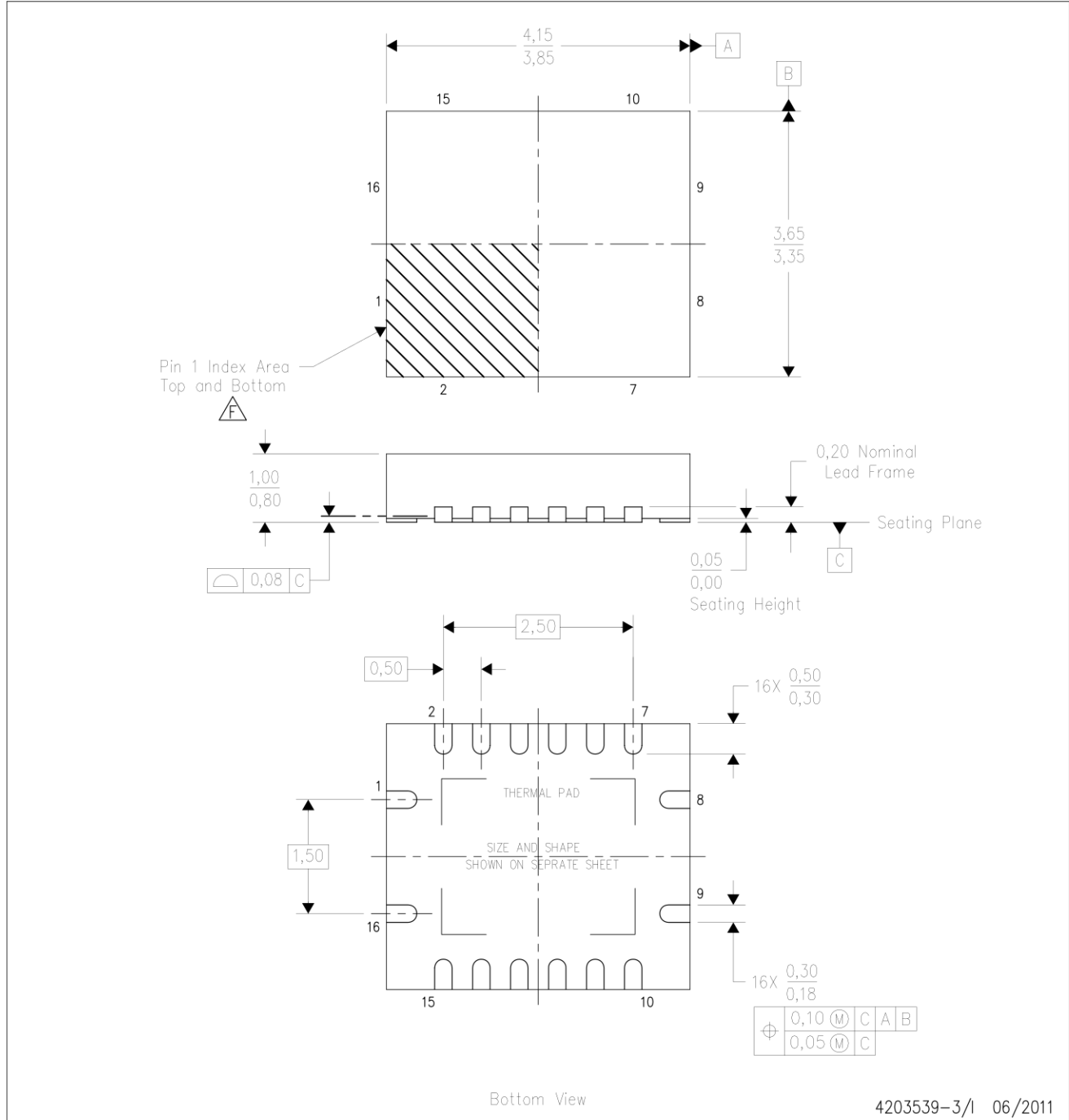


4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - G. Package complies to JEDEC MO-241 variation BA.

RGY (R-PVQFN-N16)

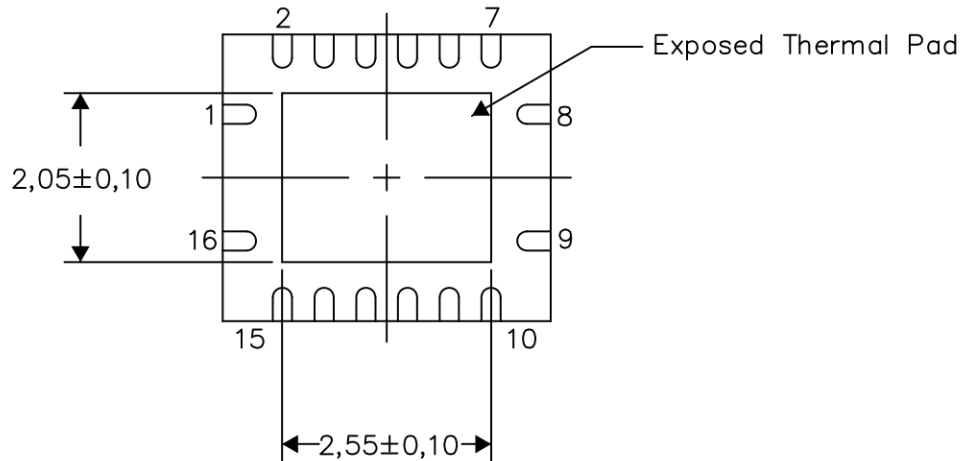
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

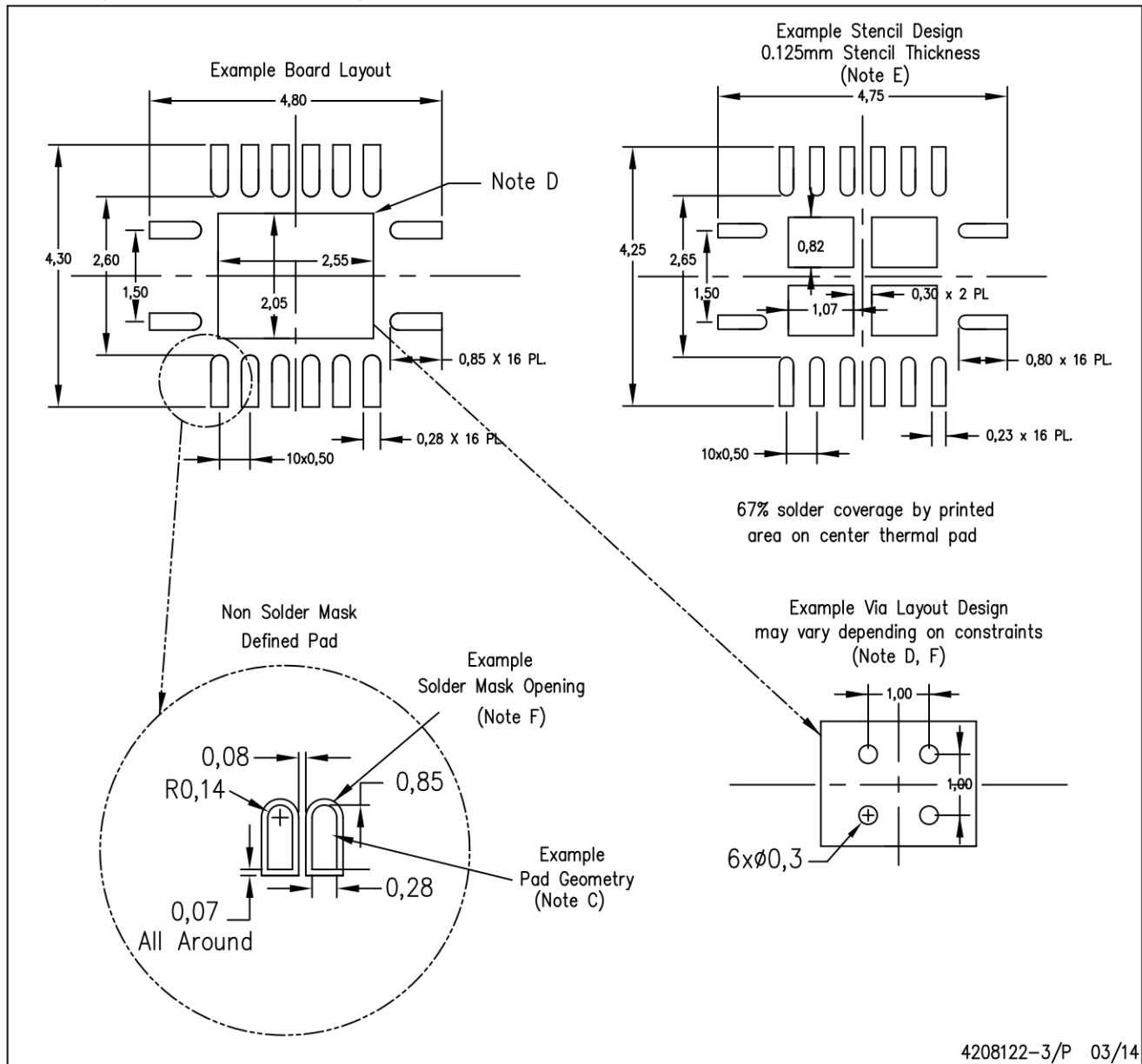
Exposed Thermal Pad Dimensions

4206353-3/P 03/14

NOTE: All linear dimensions are in millimeters

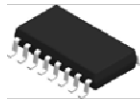
RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

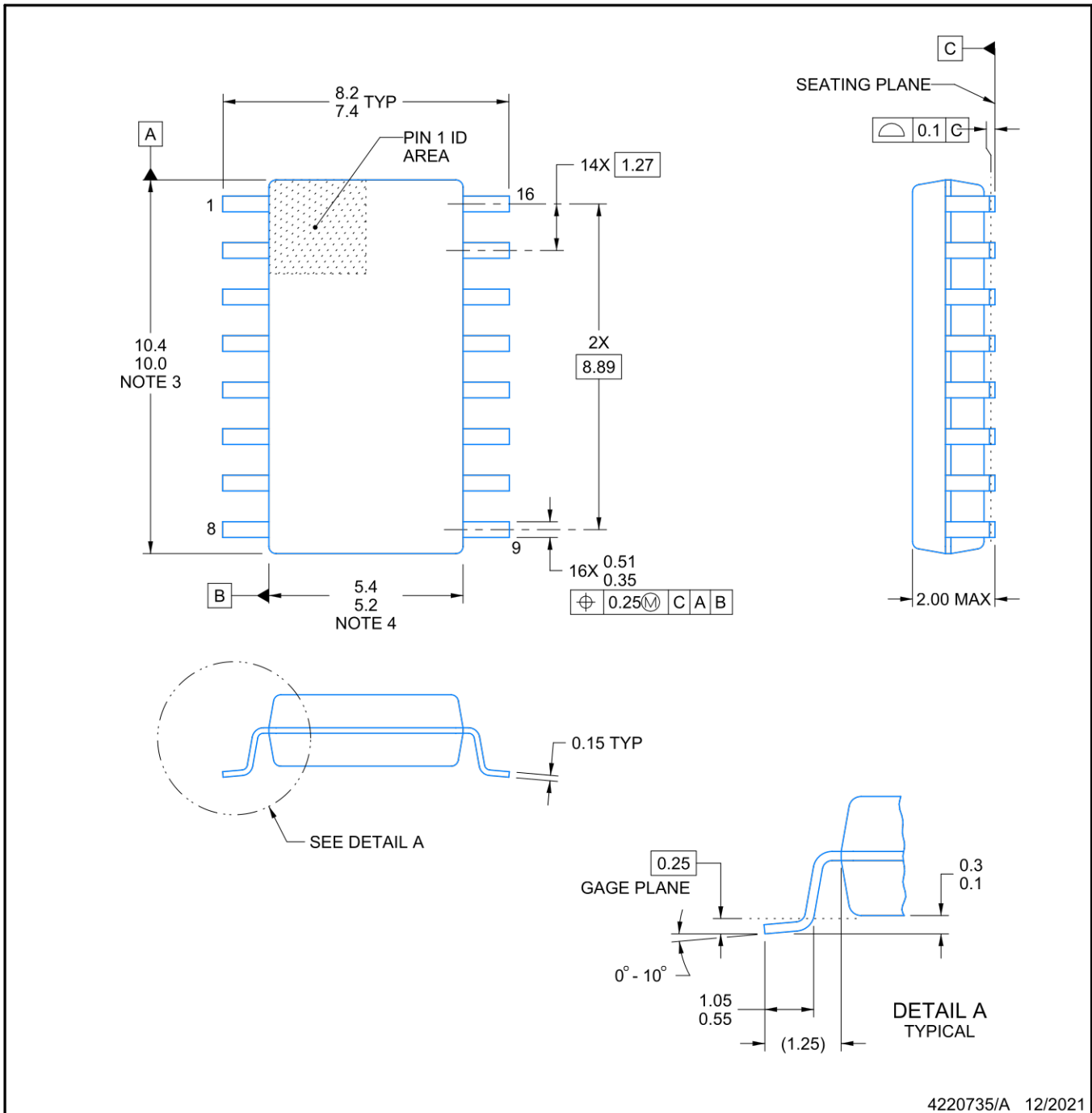
NS0016A



PACKAGE OUTLINE

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES:

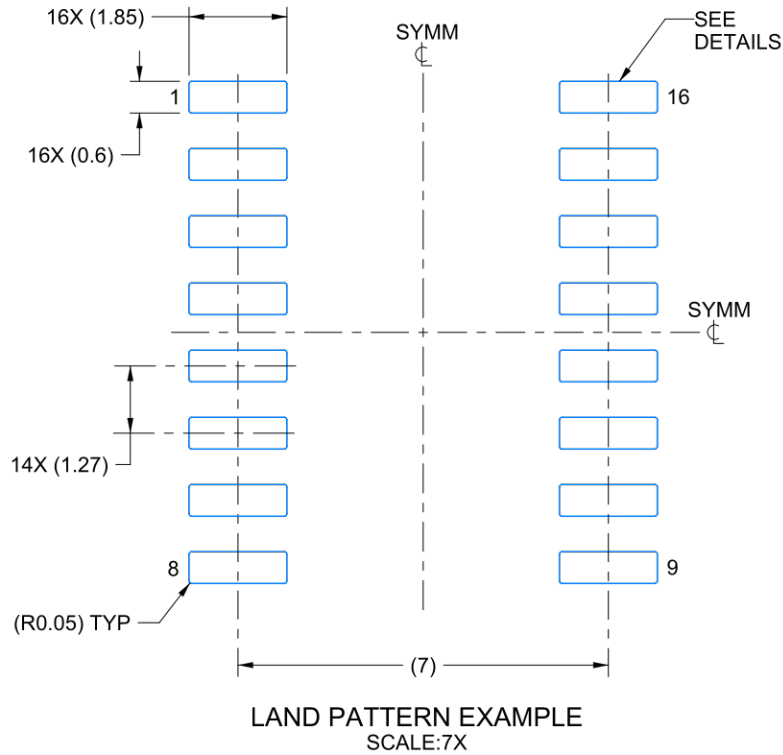
- All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

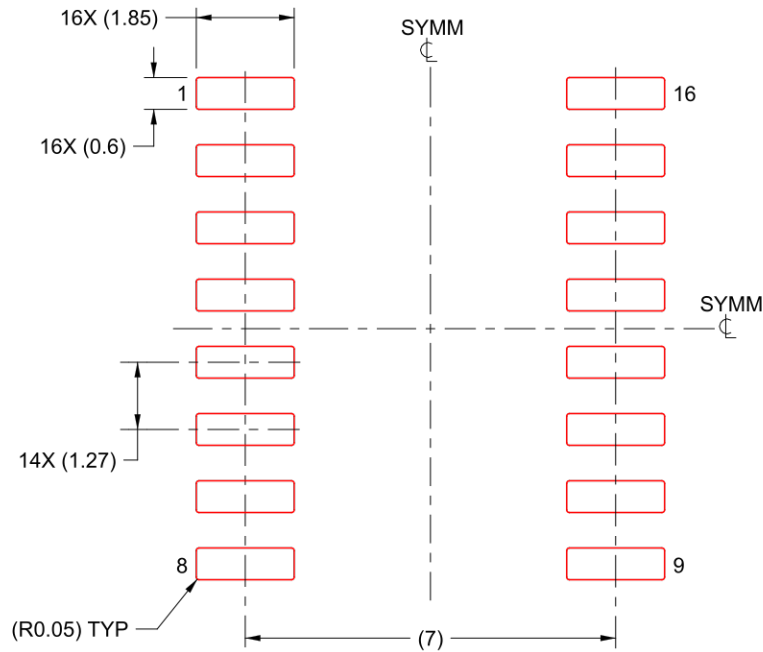
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

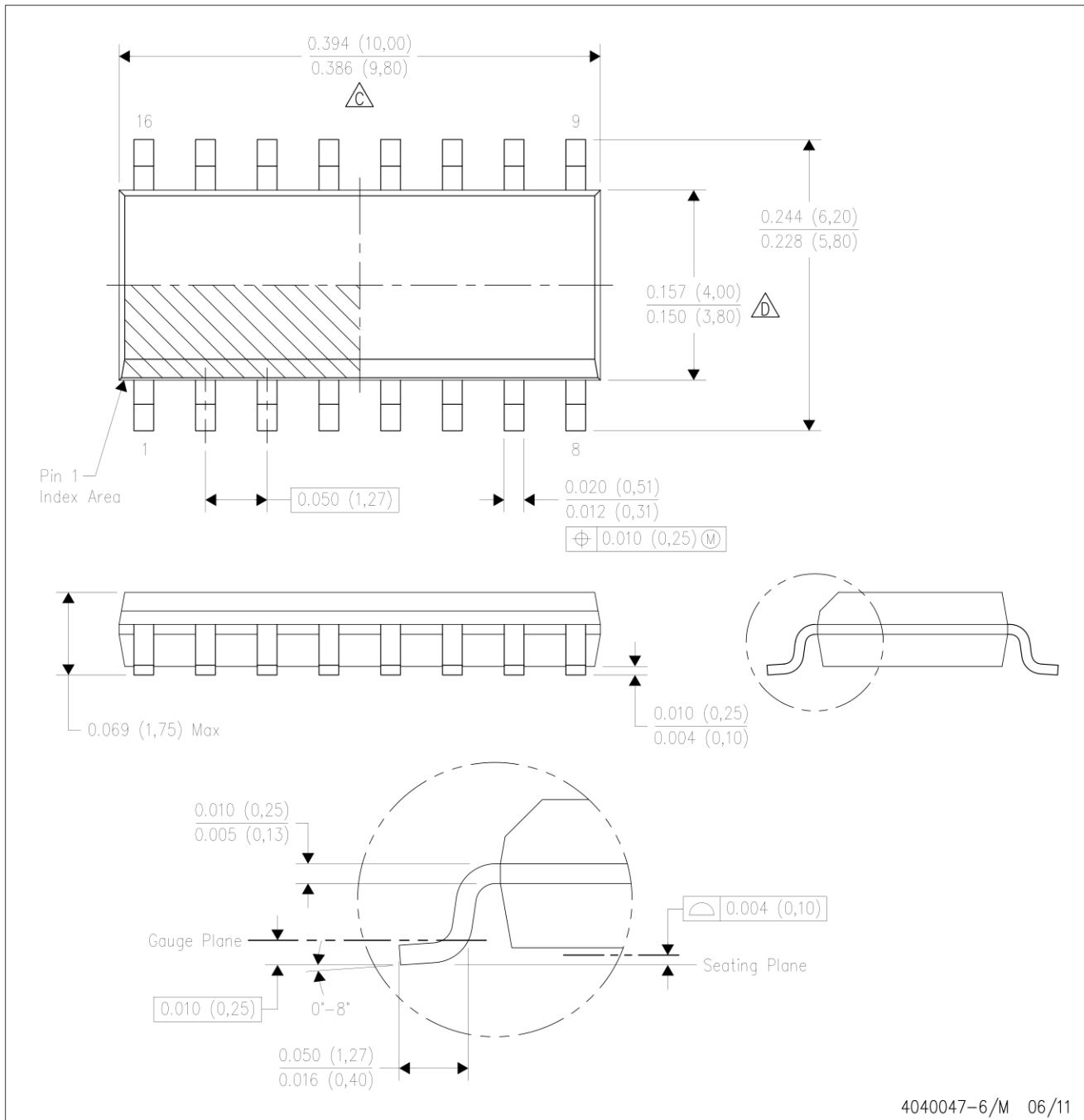
4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

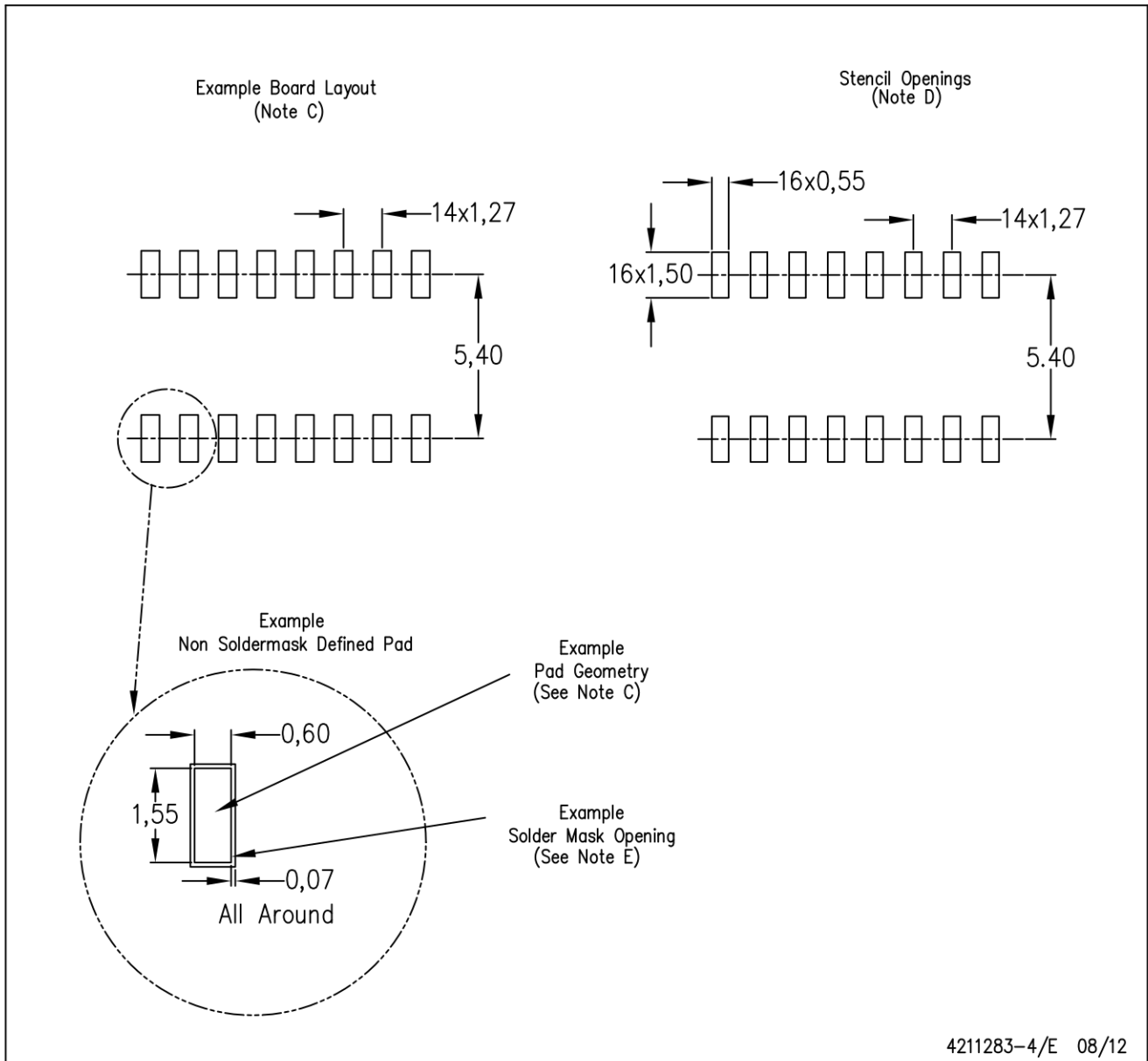
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

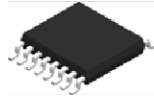
D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

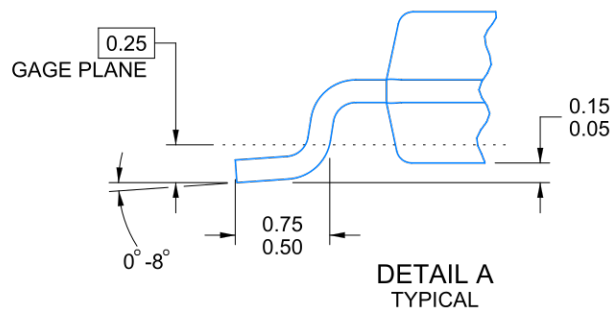
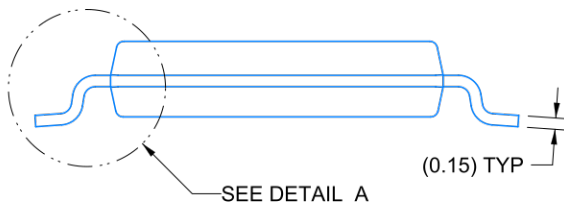
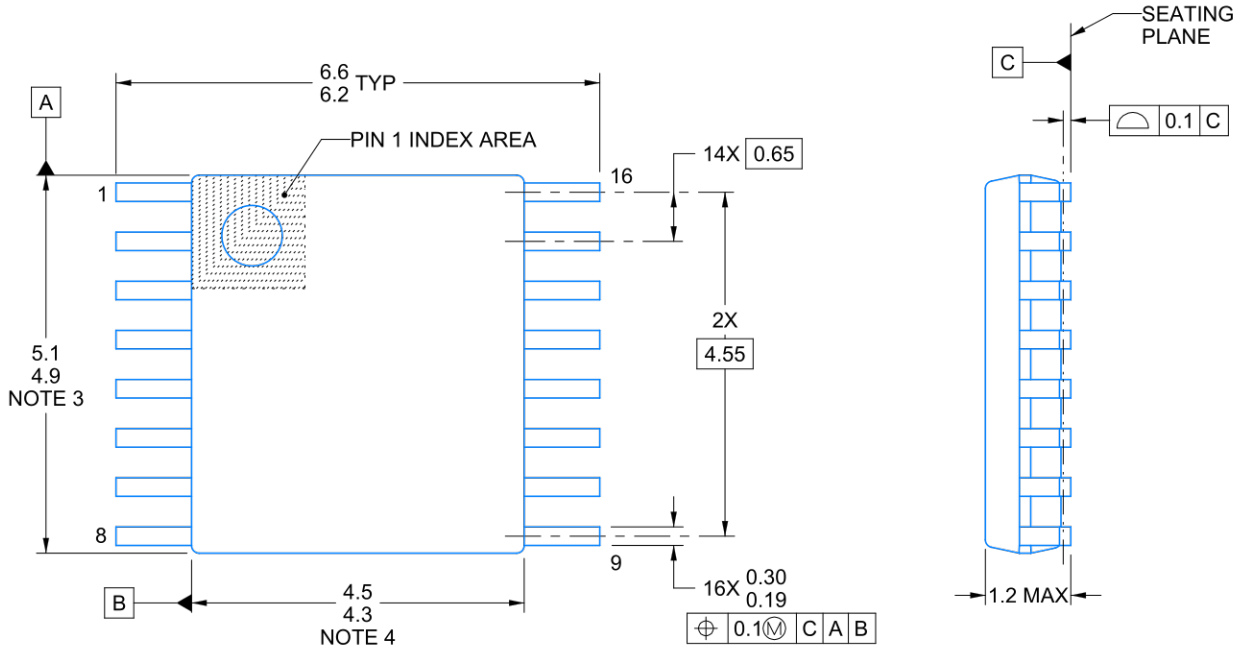
PW0016A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220204/A 02/2017

NOTES:

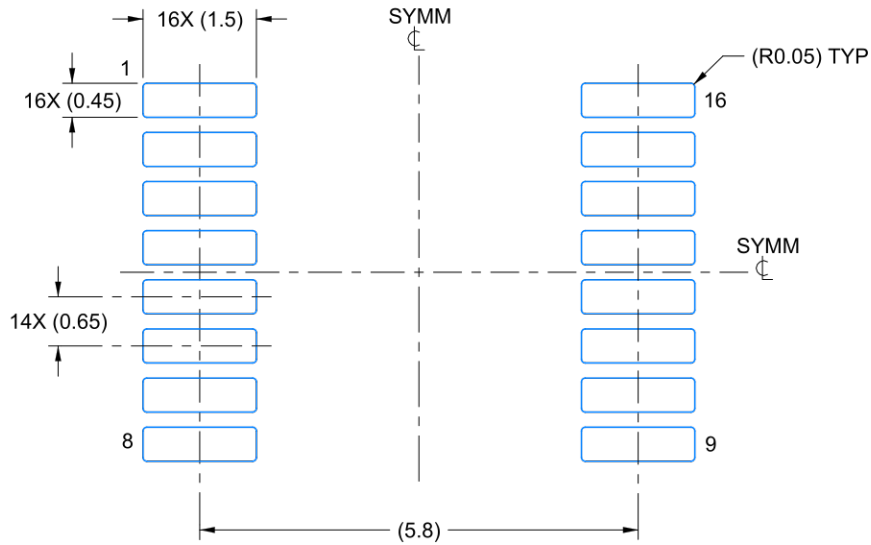
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

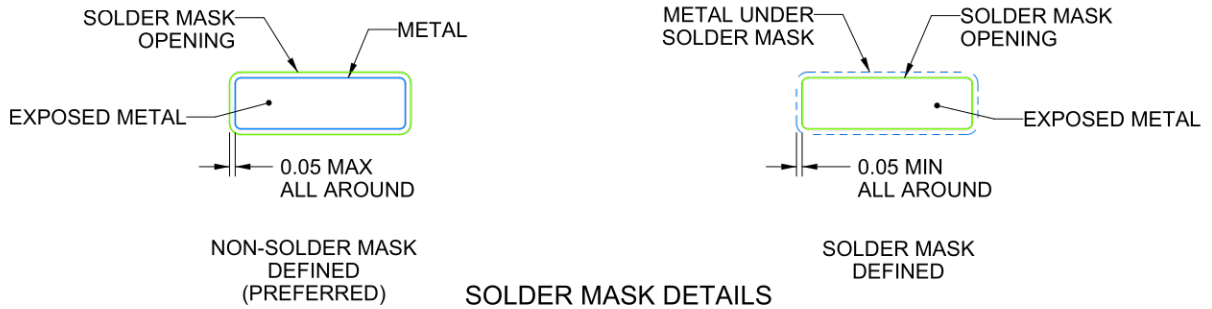
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

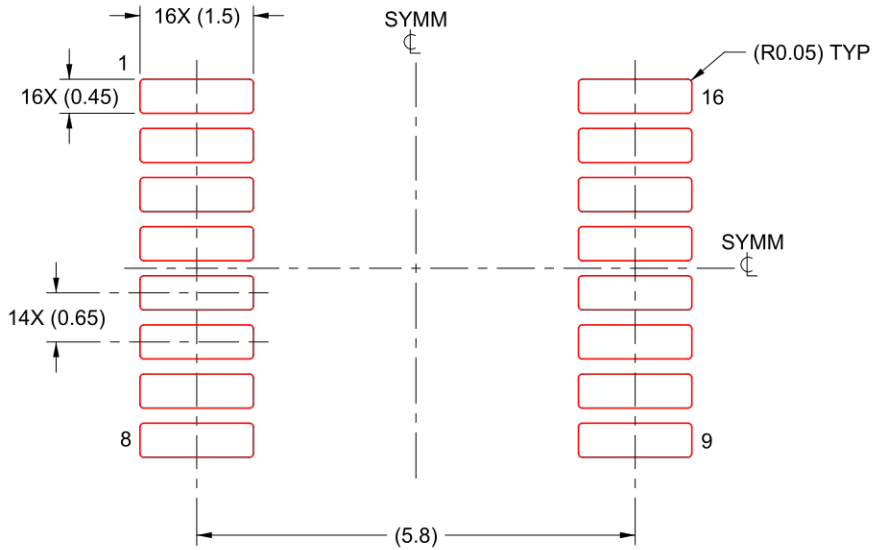
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

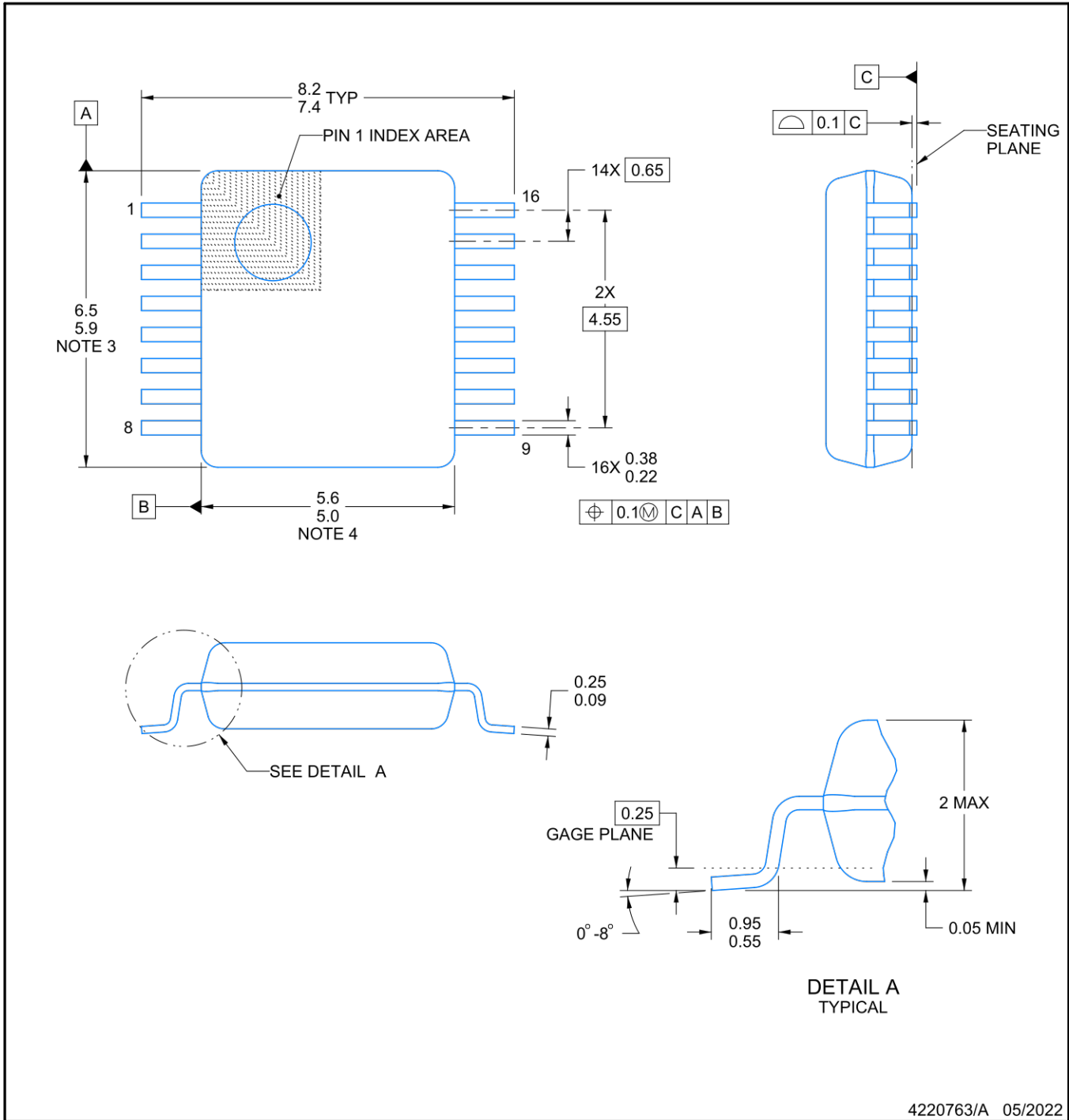
DB0016A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

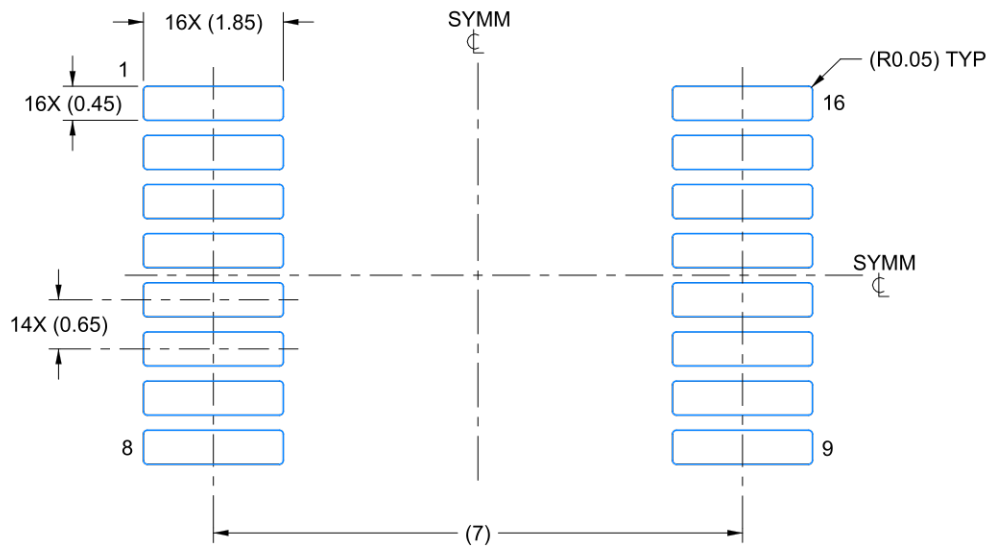
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

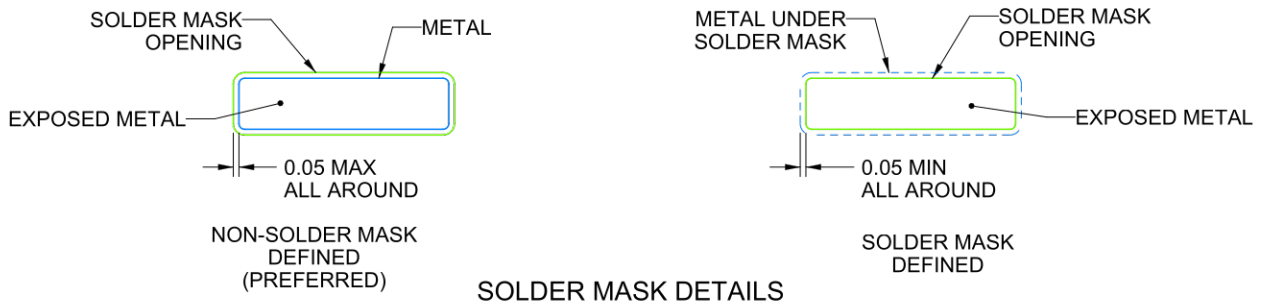
DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220763/A 05/2022

NOTES: (continued)

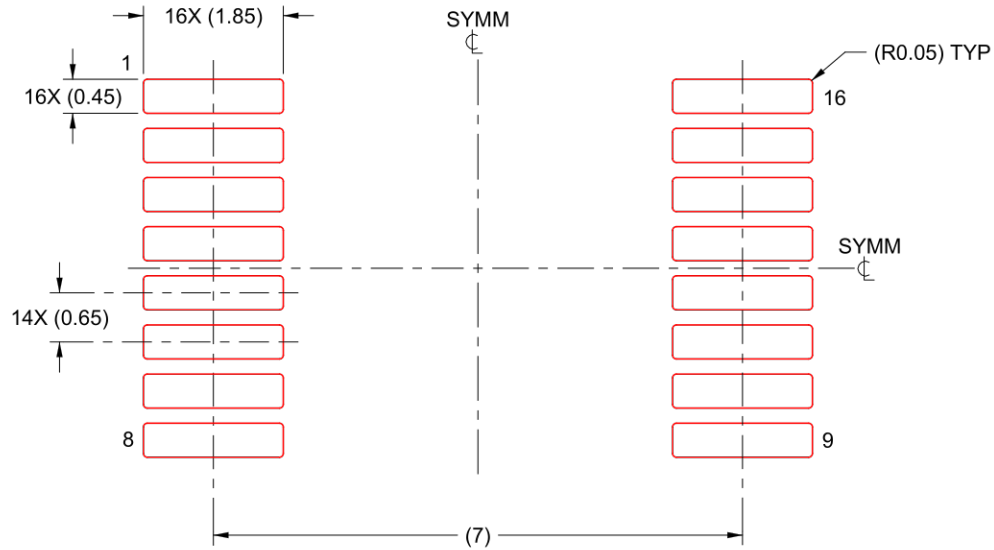
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

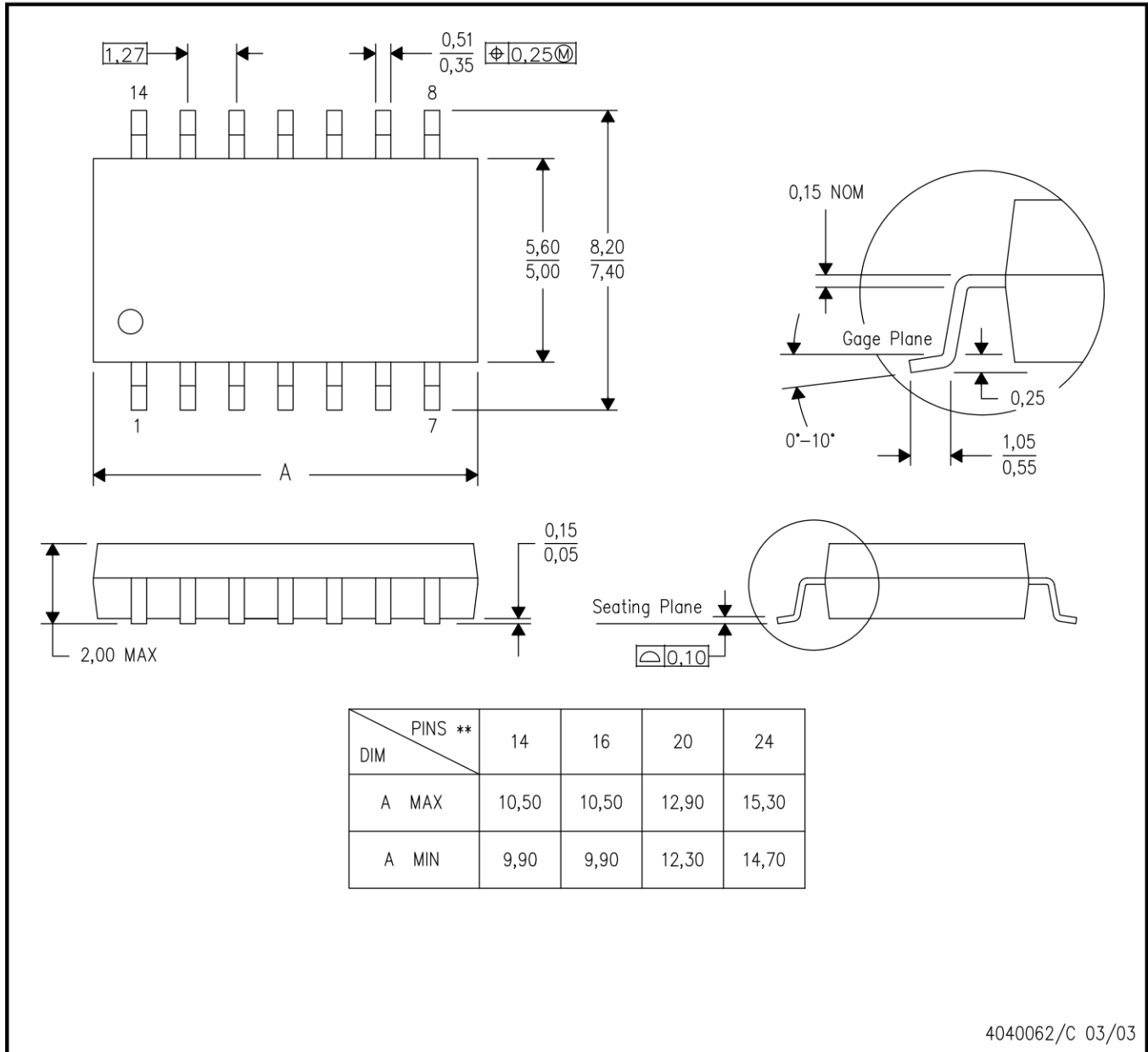
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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